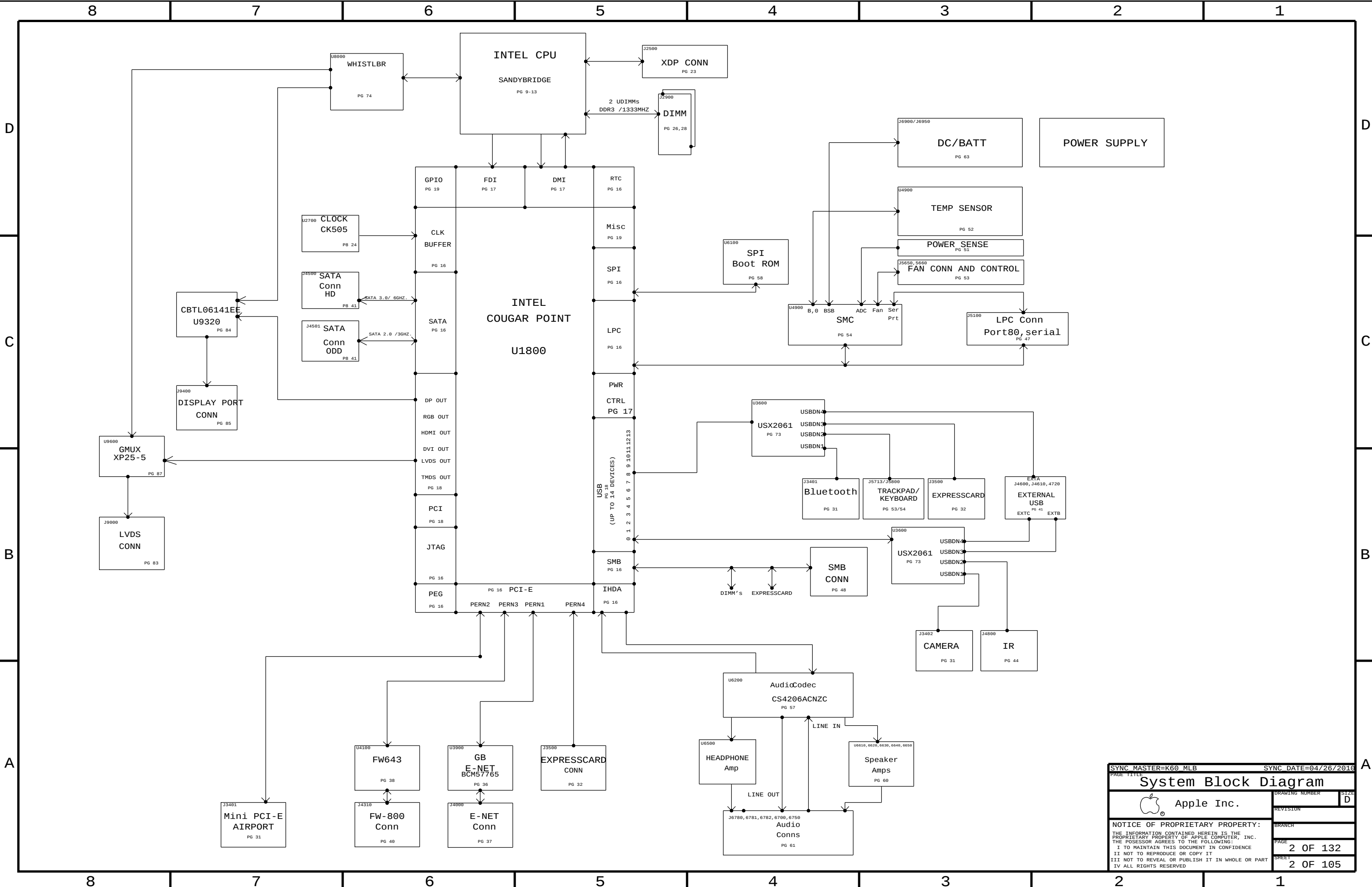
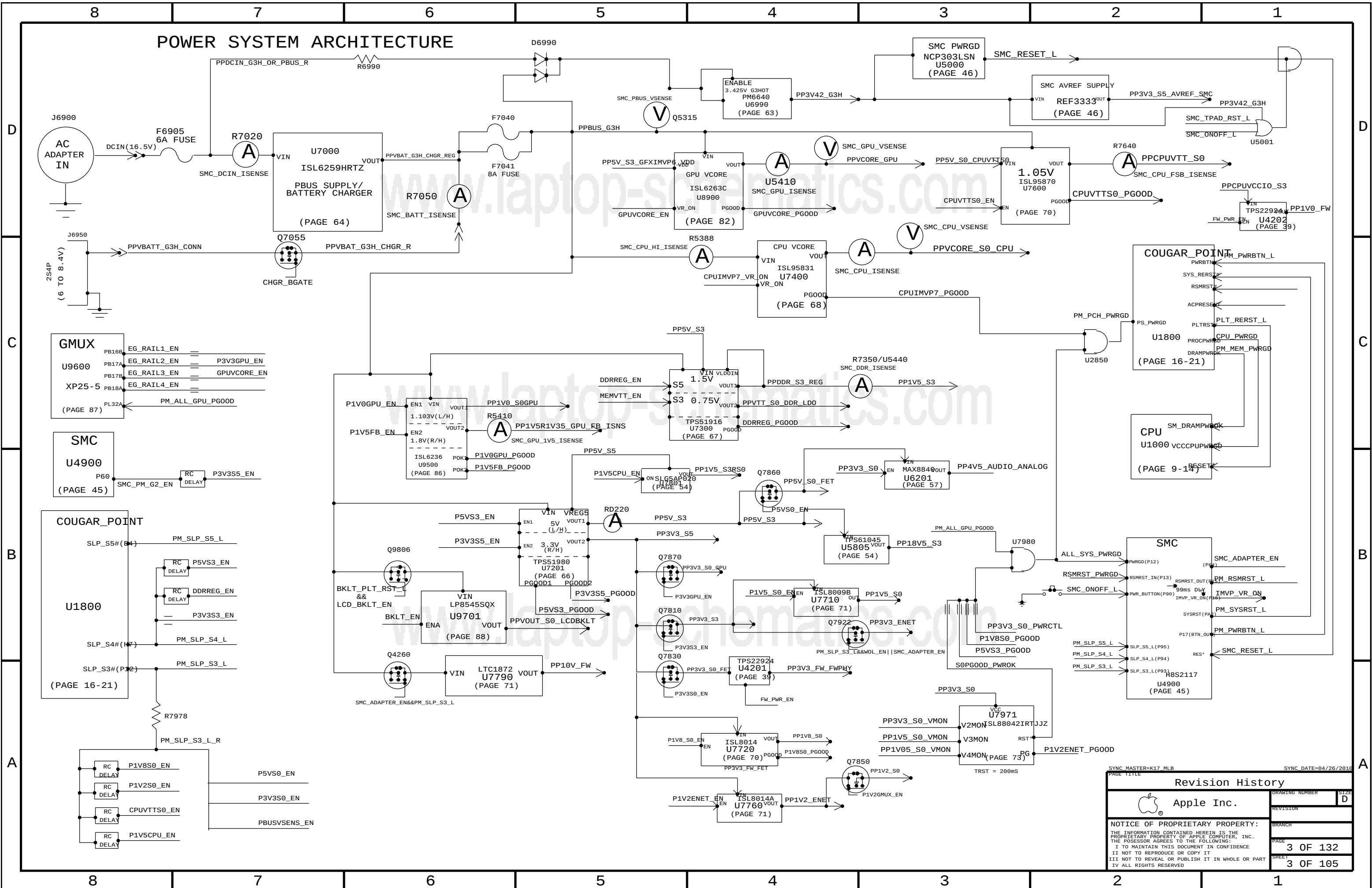
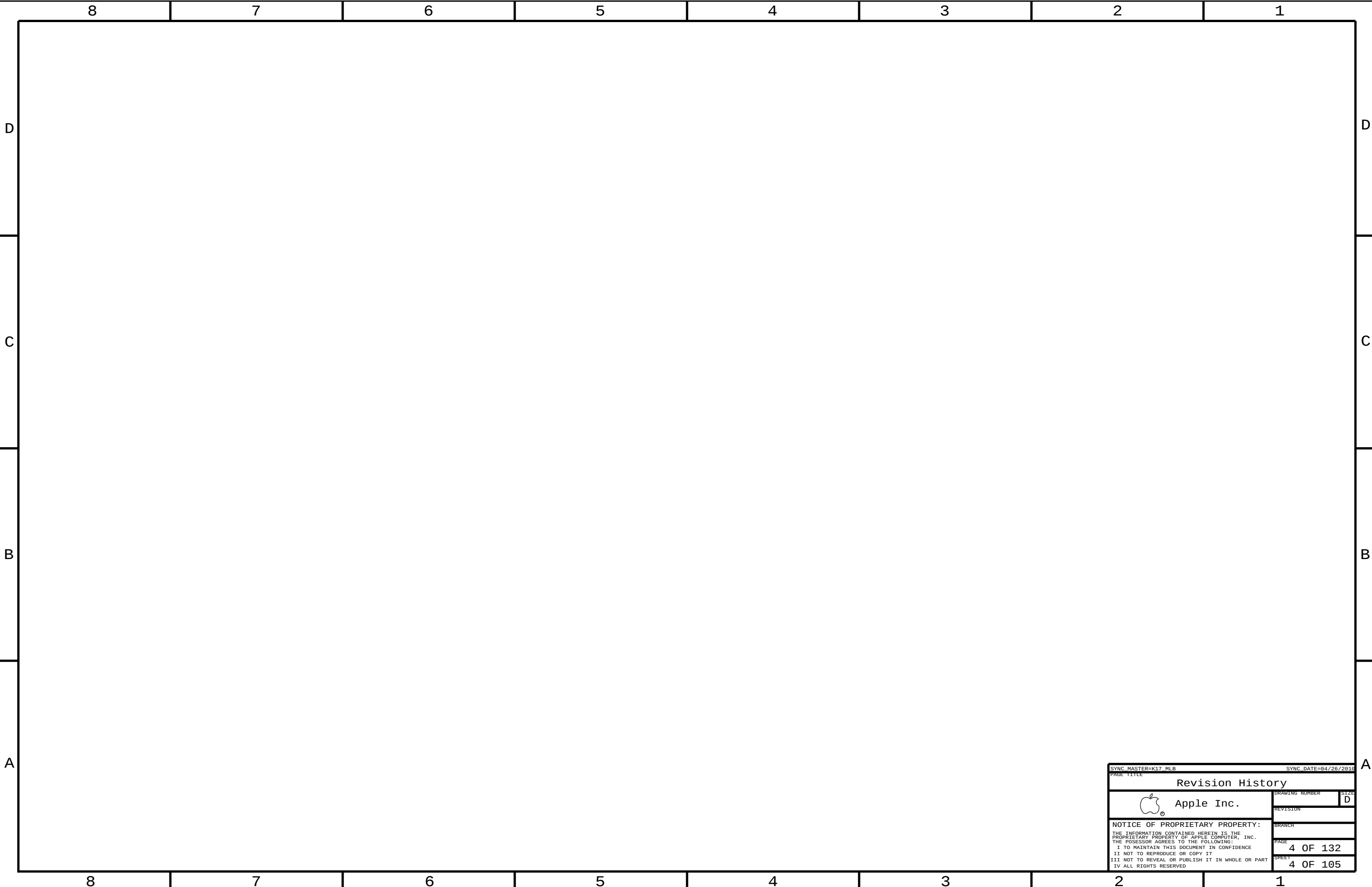




POWER SYSTEM ARCHITECTURE



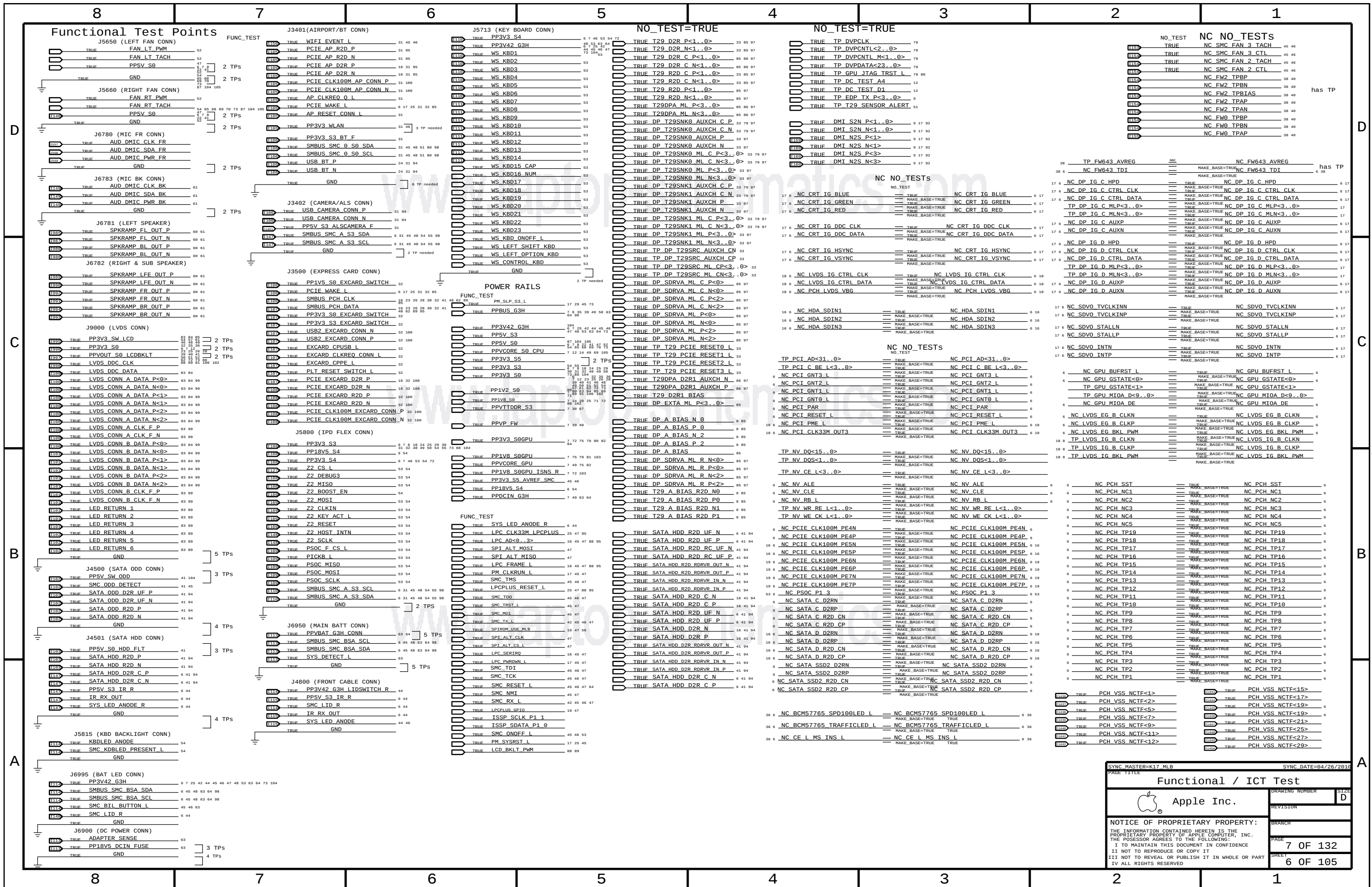
Revision History					
Apple Inc.	DRAWING NUMBER	D			
	REVISION				
	BRANCH				
	PAGE	3 OF 132			
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SHEET		3 OF 105			

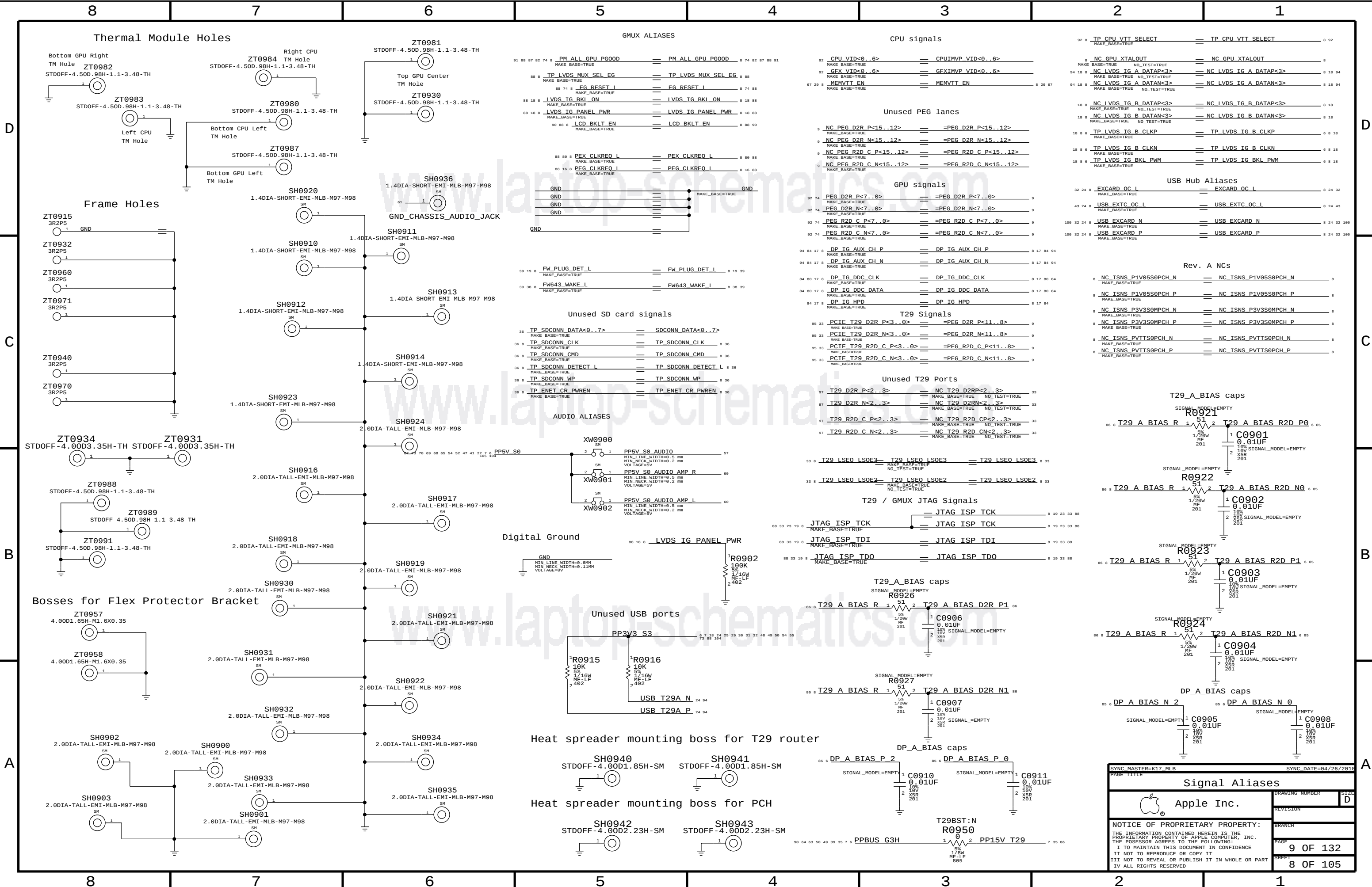


SYNC MASTER=K17_MLB

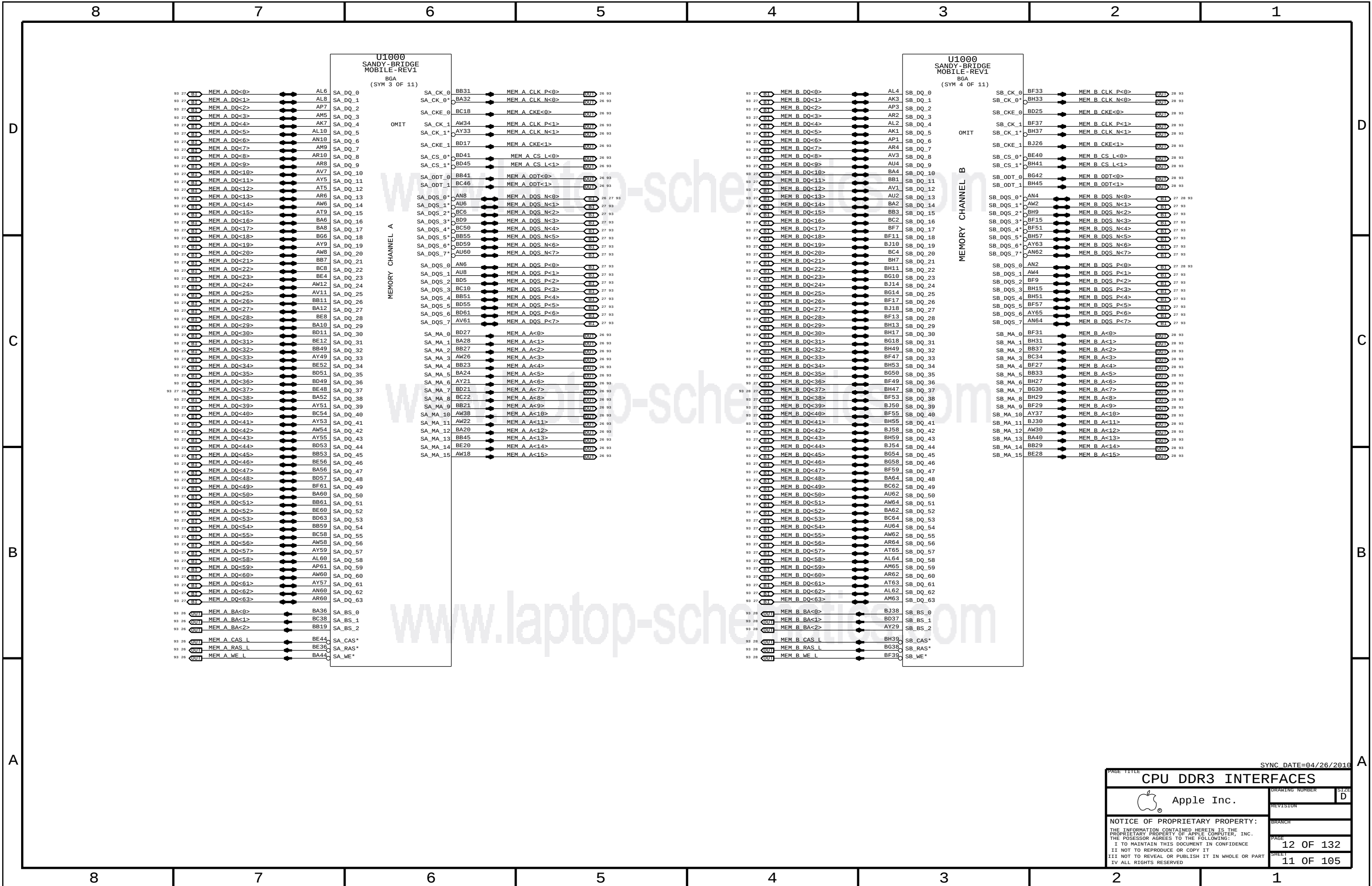
SYNC DATE=04/26/2010

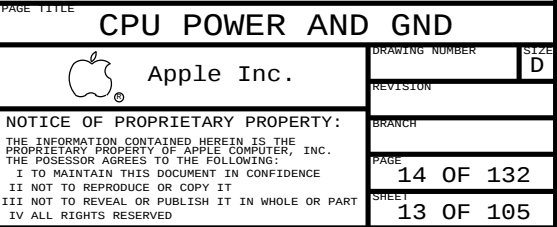
PAGE TITLE		Revision History	
 Apple Inc.		DRAWING NUMBER	SIZE D
		REVISION	
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		PAGE	4 OF 132
		SHEET	4 OF 105

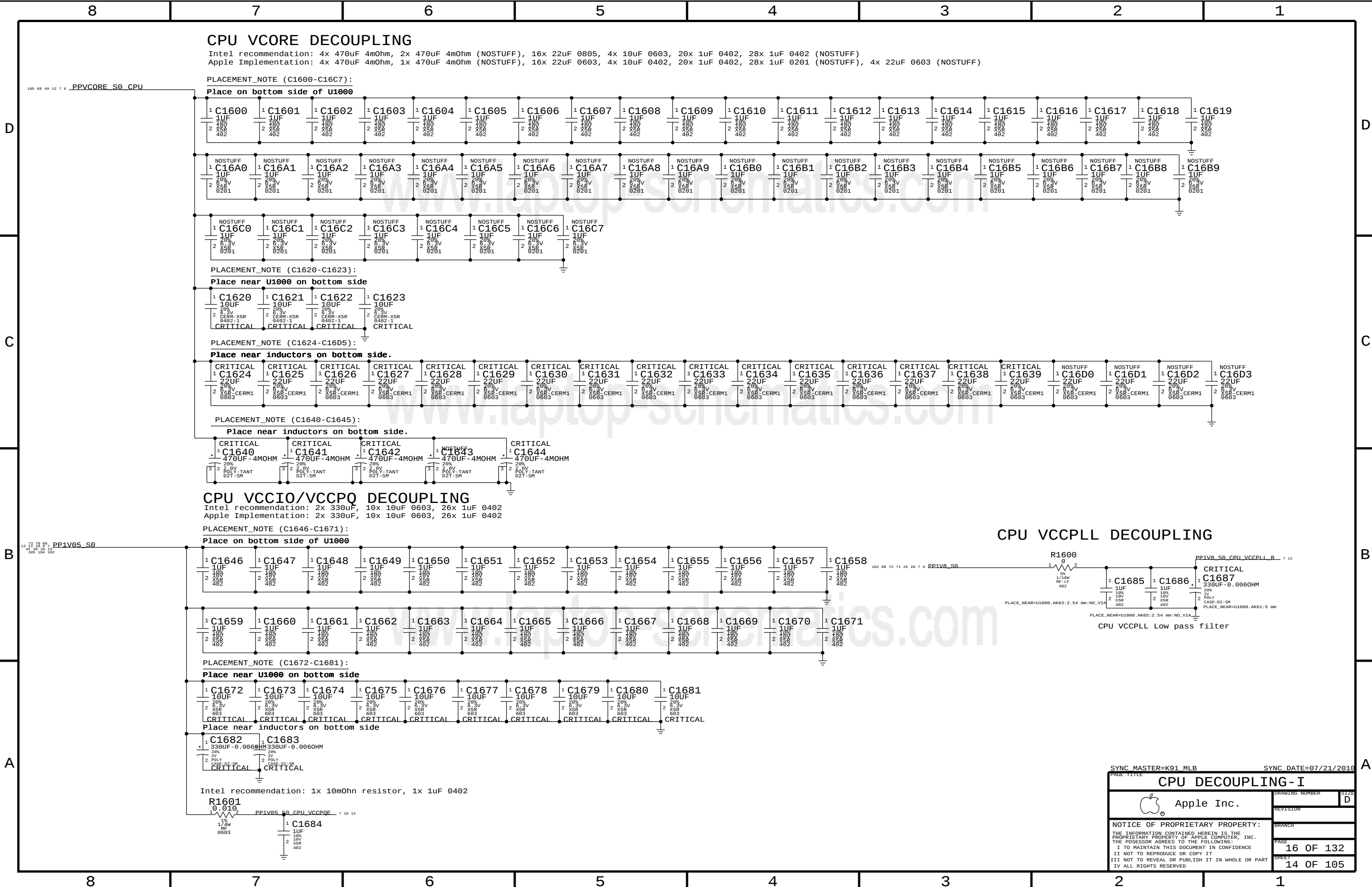




SYNC MASTER=K17_MLB		SYNC DATE=04/26/2010	
PAGE TITLE		DRAWING NUMBER	SIZE
Apple Inc.		REVISION	D
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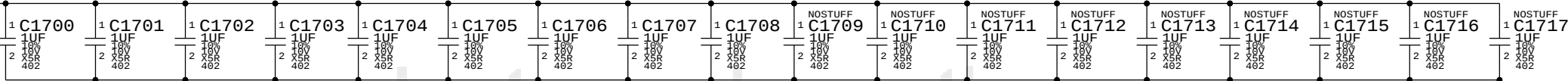


SYNC MASTER=K91 MLB		SYNC DATE=07/21/2016	
PAGE TITLE		CPU DECOUPLING-I	
 Apple Inc.		DRAWING NUMBER	SIZE
		REVISION	D
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		PAGE	16 OF 132
		SHEET	14 OF 105

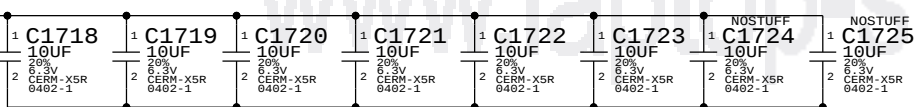
VAXG DECOUPLING

Intel recommendation: 2x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 6x 22uF 0805, 2x 22uF 0805 (NOSTUFF), 6x 10uF 0603, 2x 10uF 0603 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)
Apple Implementation: 2x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 6x 22uF 0603, 2x 22uF 0603 (NOSTUFF), 6x 10uF 0402, 2x 10uF 0402 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)

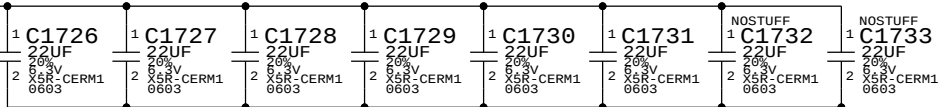
PLACEMENT_NOTE (C1700-C1708):
Place on bottom side of U1000



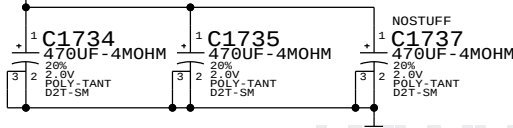
PLACEMENT_NOTE (C1718-C1723):
Place close to U1000 on bottom side



PLACEMENT_NOTE (C1726-C1731):
Place near inductors on bottom side.



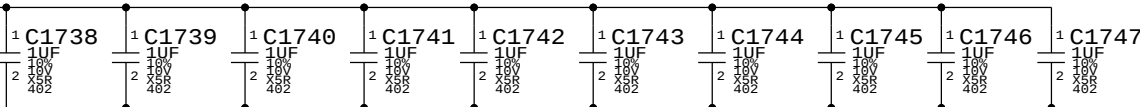
PLACEMENT_NOTE (C1734-C1735):
Place near inductors on bottom side.



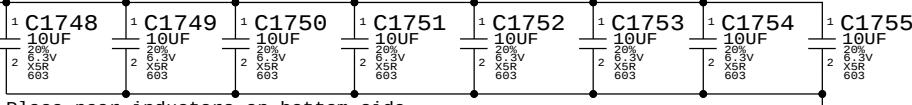
CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402

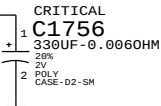
PLACEMENT_NOTE (C1738-C1747):
Place on bottom side of U1000



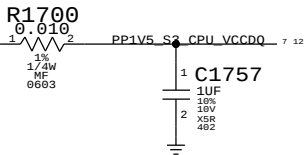
Place close to U1000 on bottom side



Place near inductors on bottom side



Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402

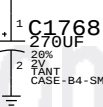
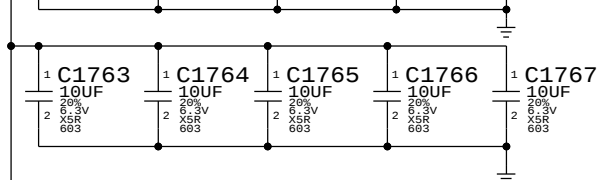
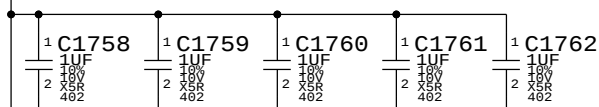


CPU VCCSA DECOUPLING

Intel recommendation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402
Apple Implementation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402

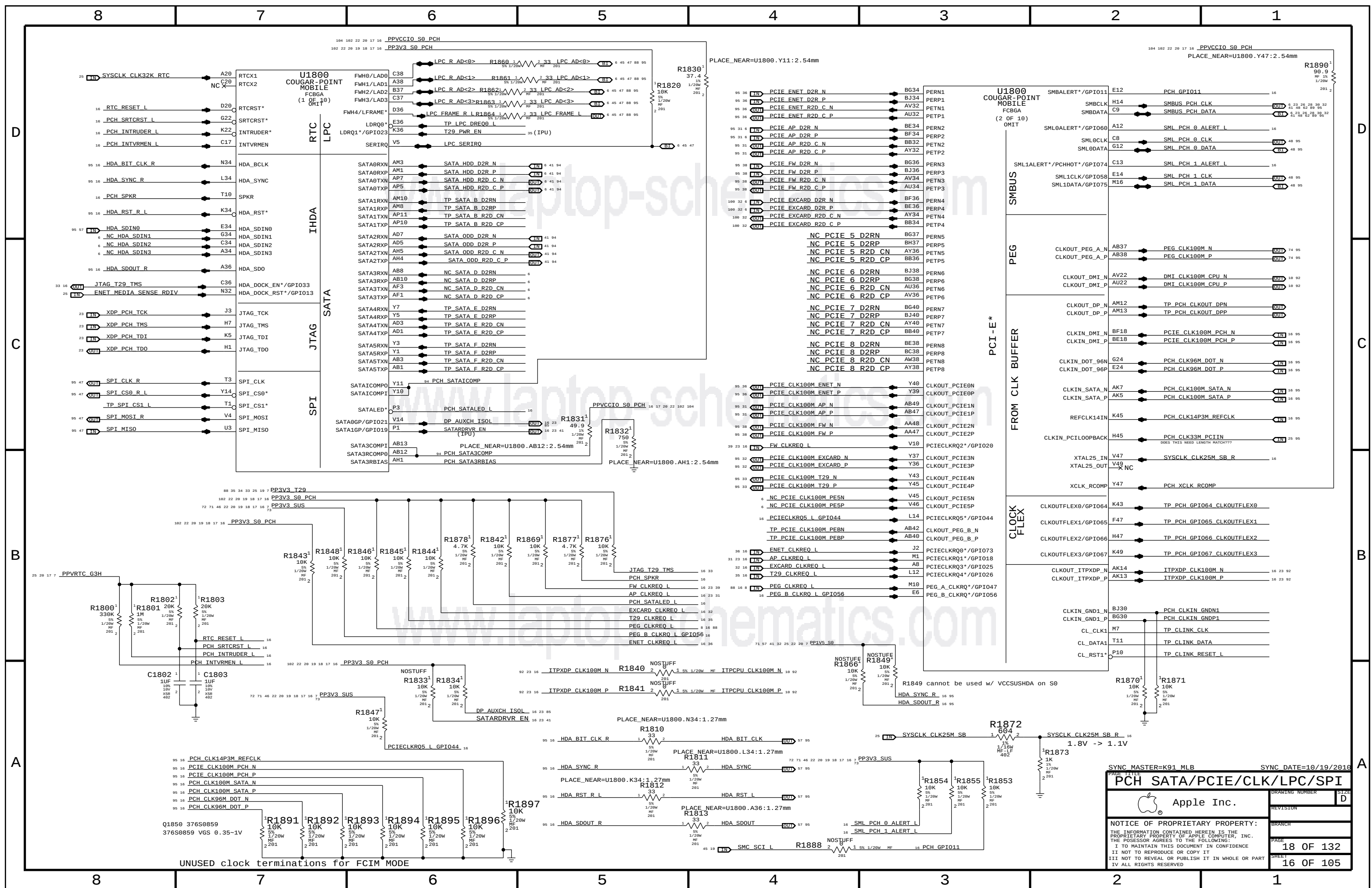
PLACEMENT_NOTE (C1758-C1762):

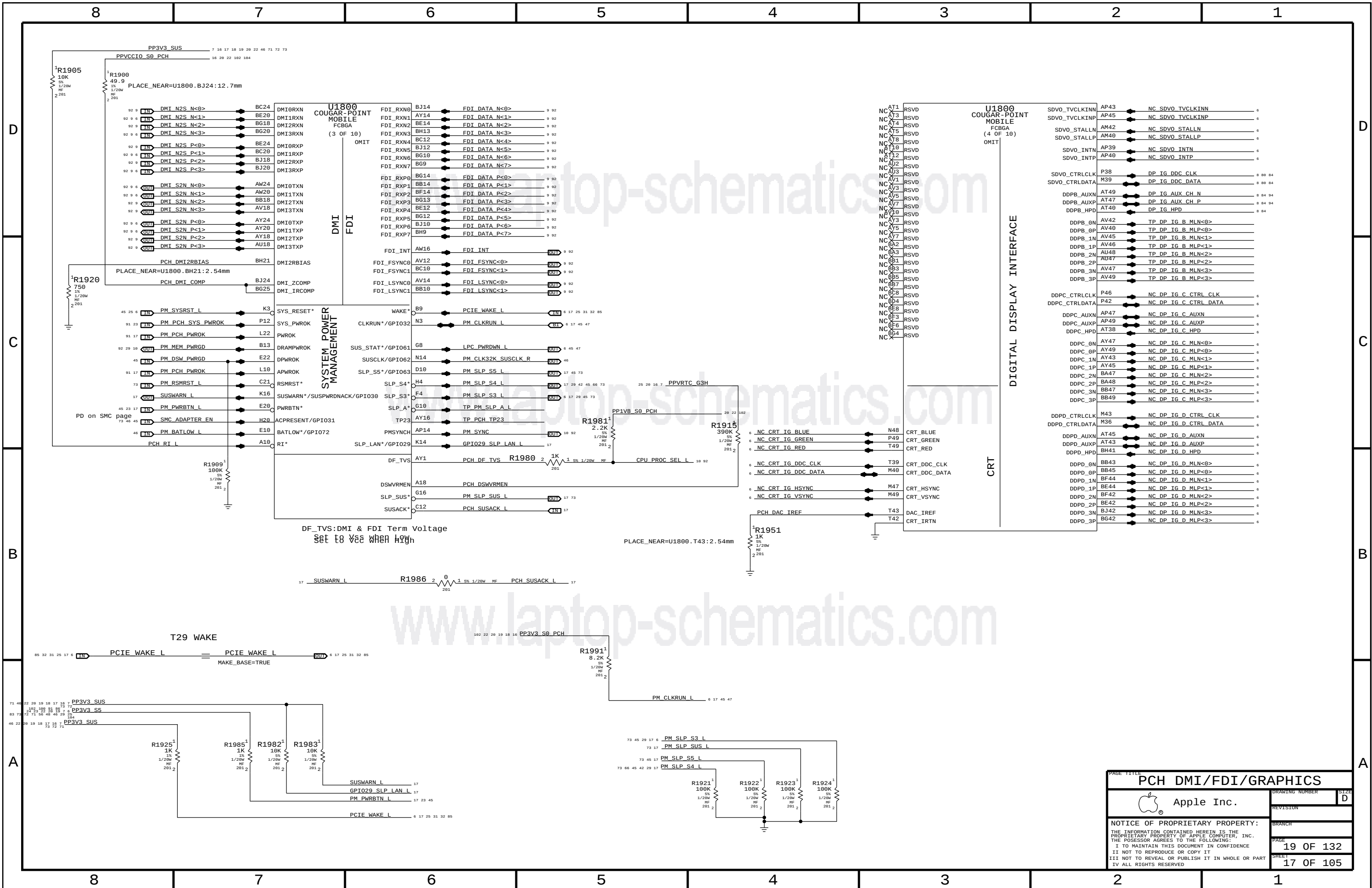
Place on bottom side of U1000

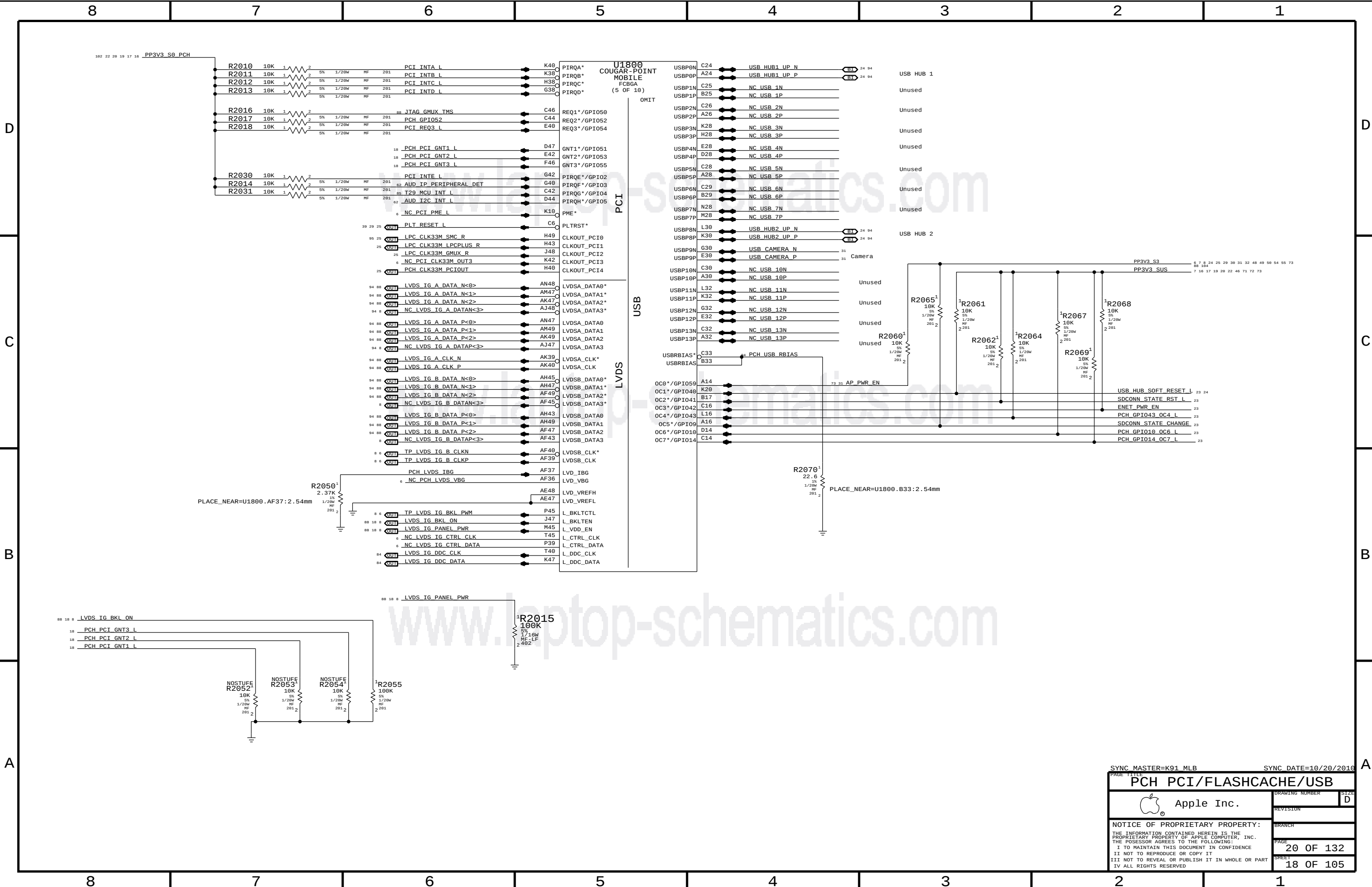


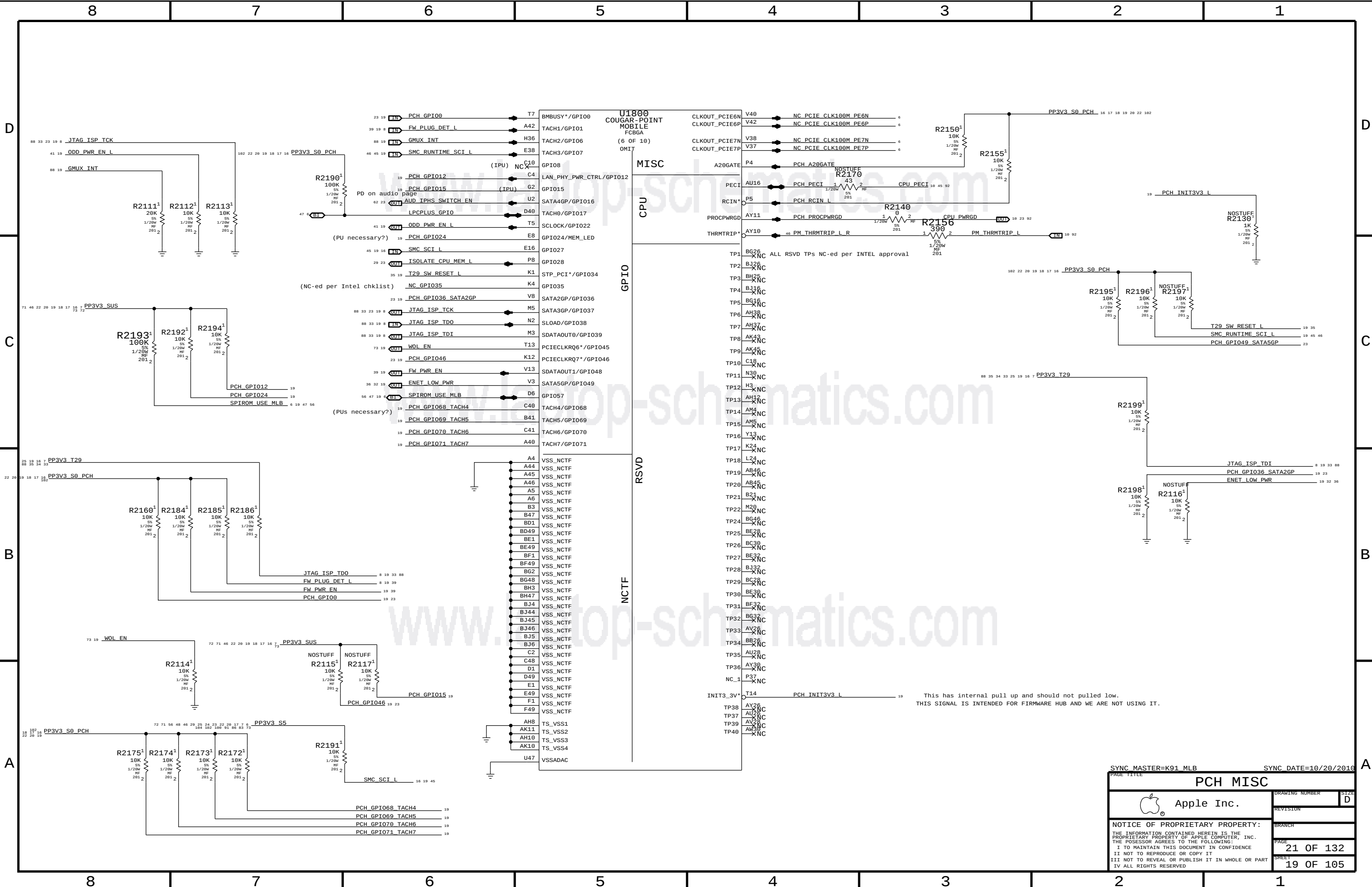
SYNC_MASTER=K91_MLB SYNC_DATE=07/21/2016

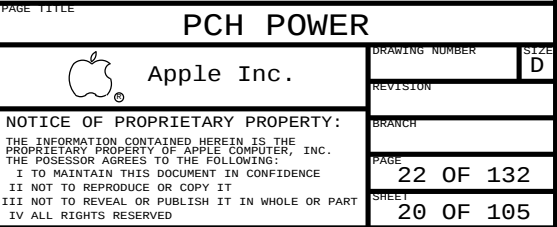
PAGE TITLE		DRAWING NUMBER	
CPU DECOUPLING-II		D	
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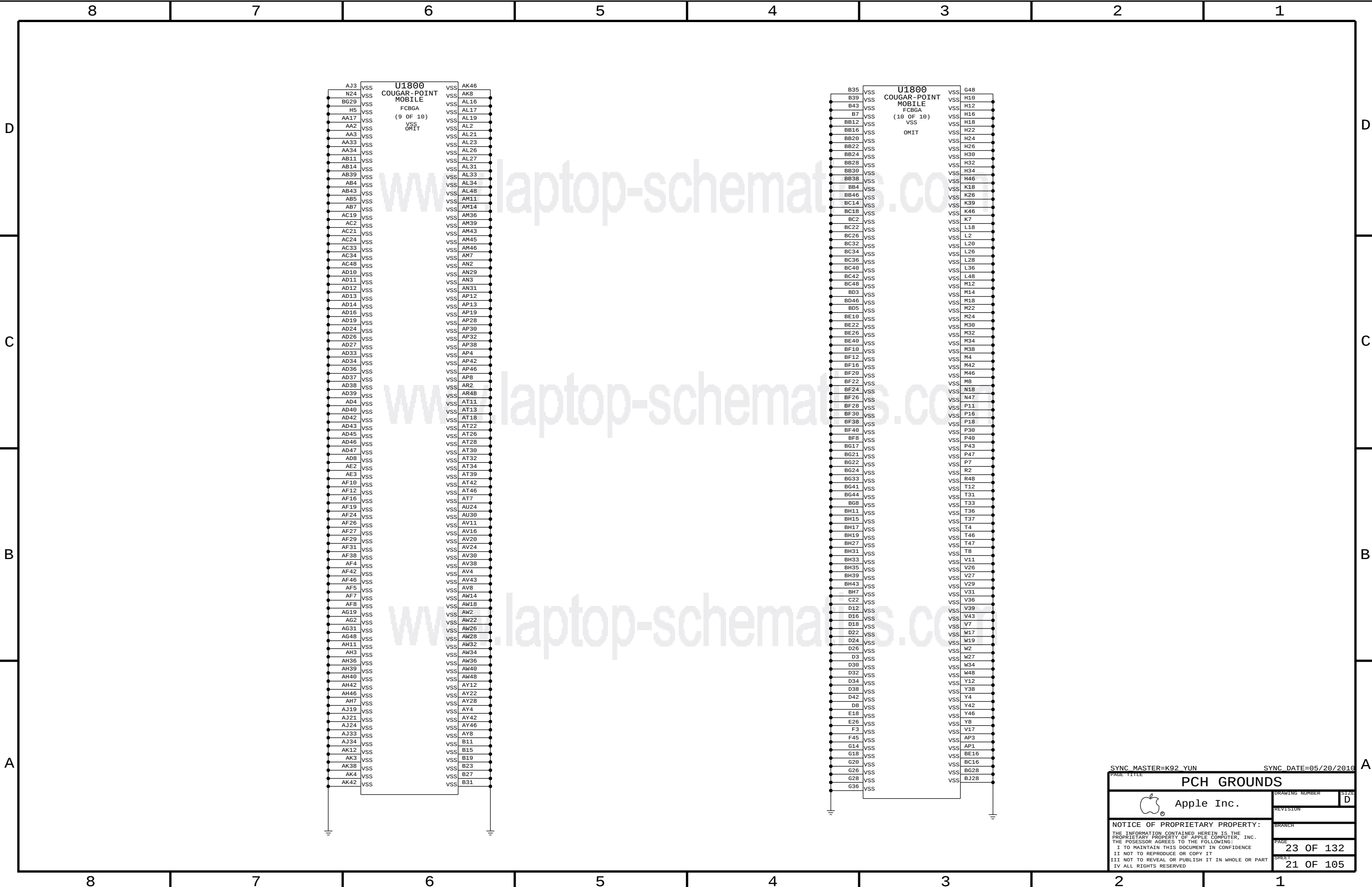


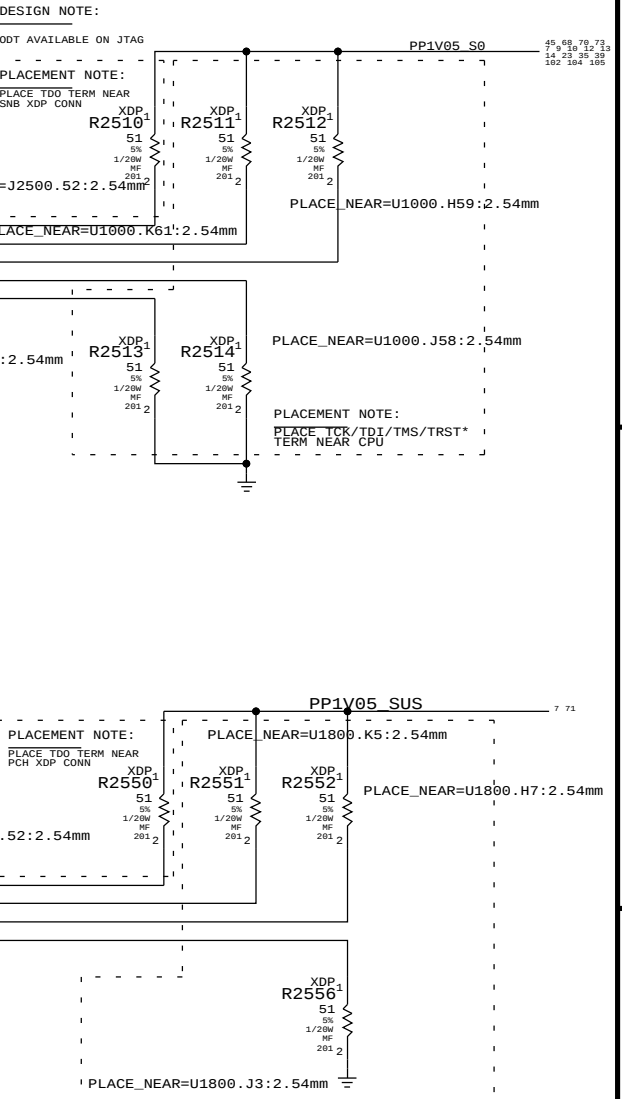
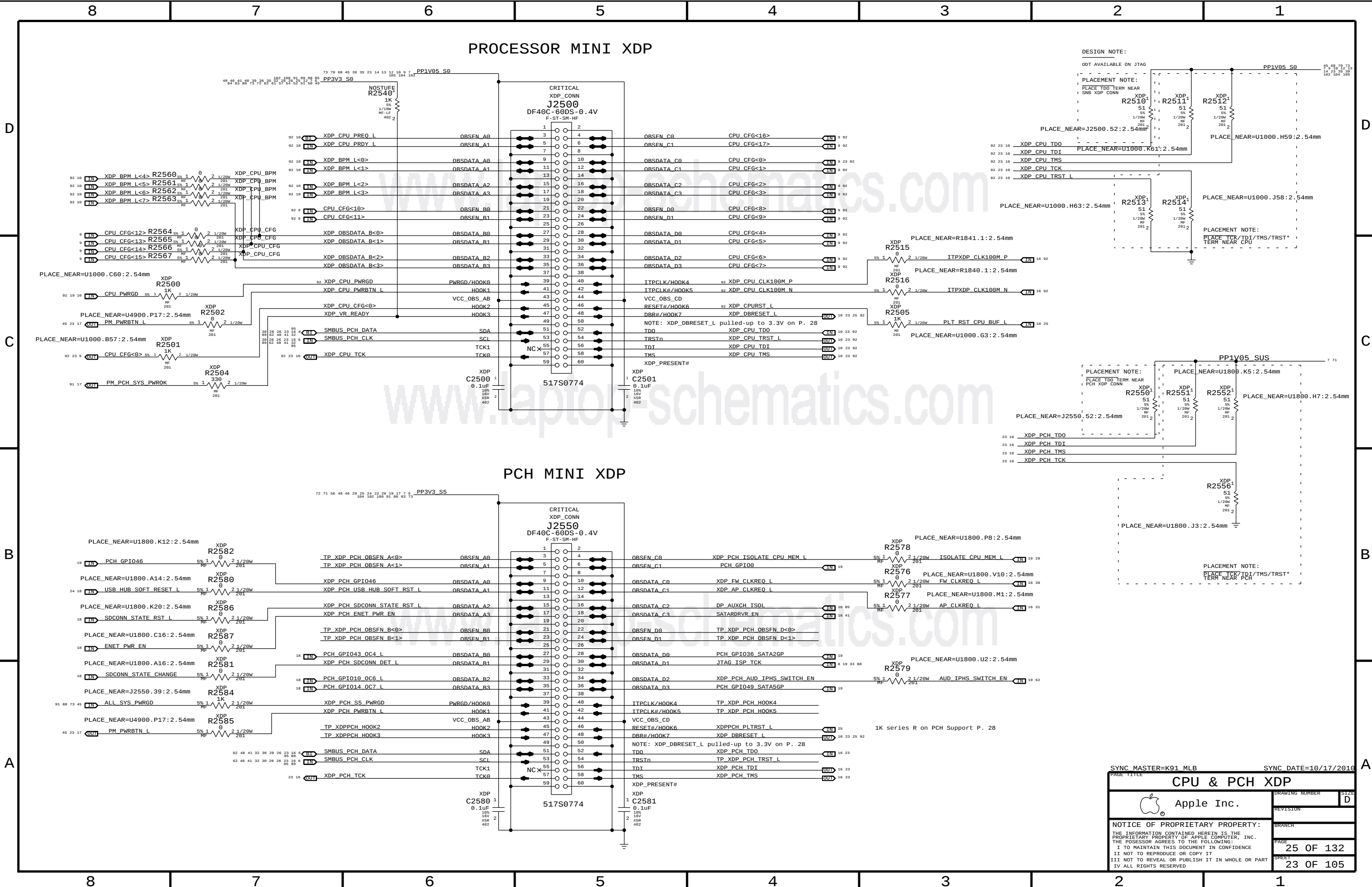




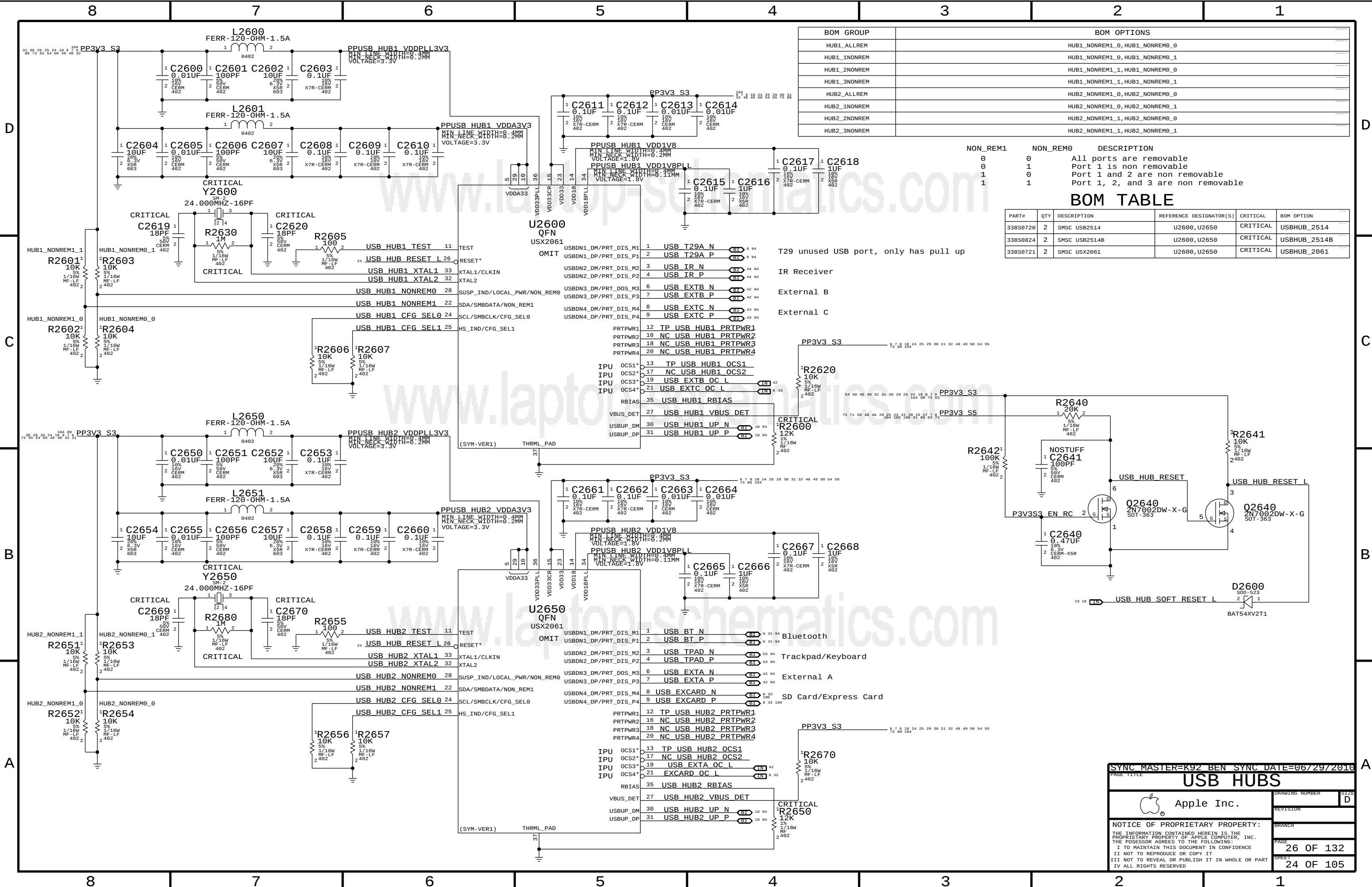








SYNC MASTER=K91 MLB		SYNC DATE=10/17/2016	
PAGE TITLE		CPU & PCH XDP	
Apple Inc.		DRAWING NUMBER	SIZE D
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BOM GROUP		BOM OPTIONS	
HUB1_ALLREM		HUB1_NONREM1_0, HUB1_NONREM0_0	
HUB1_1NONREM		HUB1_NONREM1_0, HUB1_NONREM0_1	
HUB1_2NONREM		HUB1_NONREM1_1, HUB1_NONREM0_0	
HUB1_3NONREM		HUB1_NONREM1_1, HUB1_NONREM0_1	
HUB2_ALLREM		HUB2_NONREM1_0, HUB2_NONREM0_0	
HUB2_1NONREM		HUB2_NONREM1_0, HUB2_NONREM0_1	
HUB2_2NONREM		HUB2_NONREM1_1, HUB2_NONREM0_0	
HUB2_3NONREM		HUB2_NONREM1_1, HUB2_NONREM0_1	

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U2600, U2650	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U2600, U2650	CRITICAL	USBHUB_2514B
338S0721	2	SMSC USX2061	U2600, U2650	CRITICAL	USBHUB_2061

T29 unused USB port, only has pull up

IR Receiver

External B

External C

Bluetooth

Trackpad/Keyboard

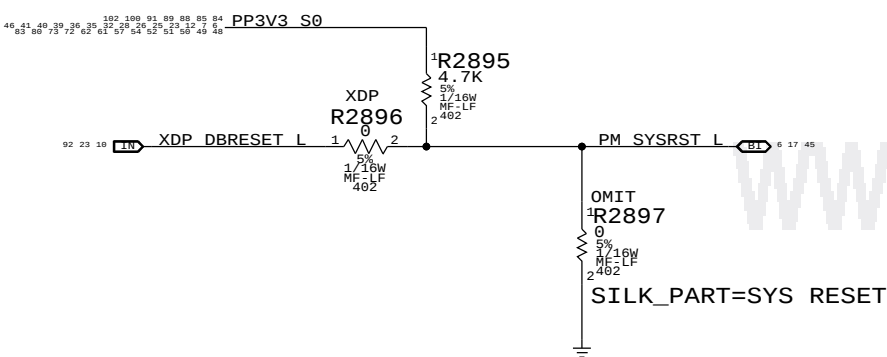
External A

SD Card/Express Card

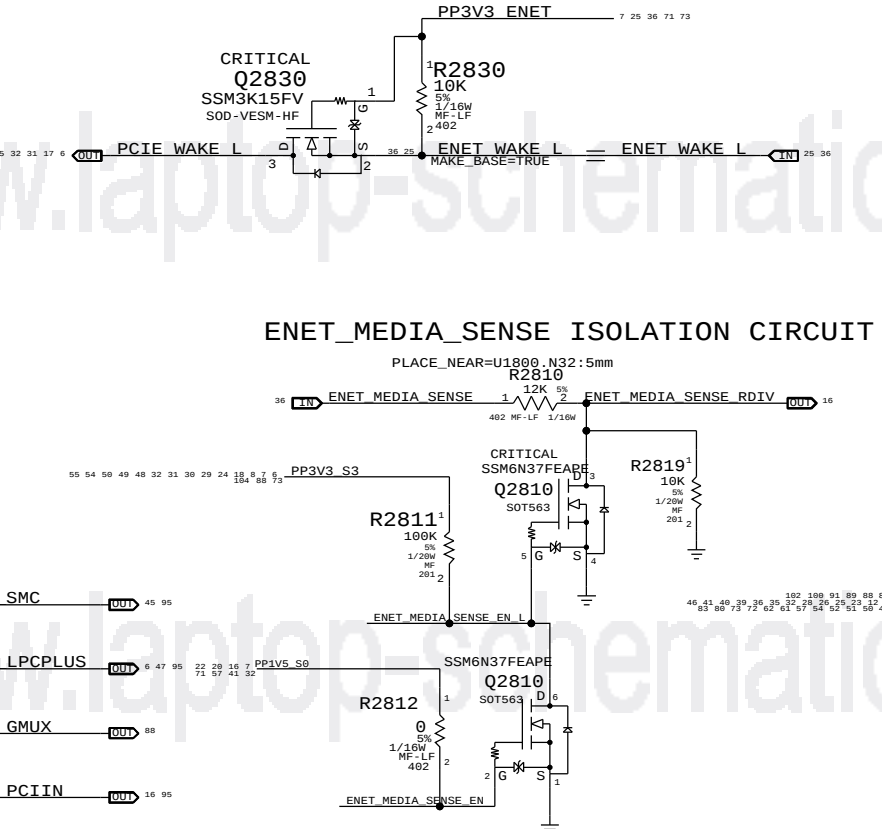
SYNC MASTER=K92 BEN SYNC DATE=06/29/2010

PAGE TITLE		PAGE	
USB HUBS		26 OF 132	
Apple Inc.		24 OF 105	
DRAWING NUMBER		REVISION	
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PCH Reset Button

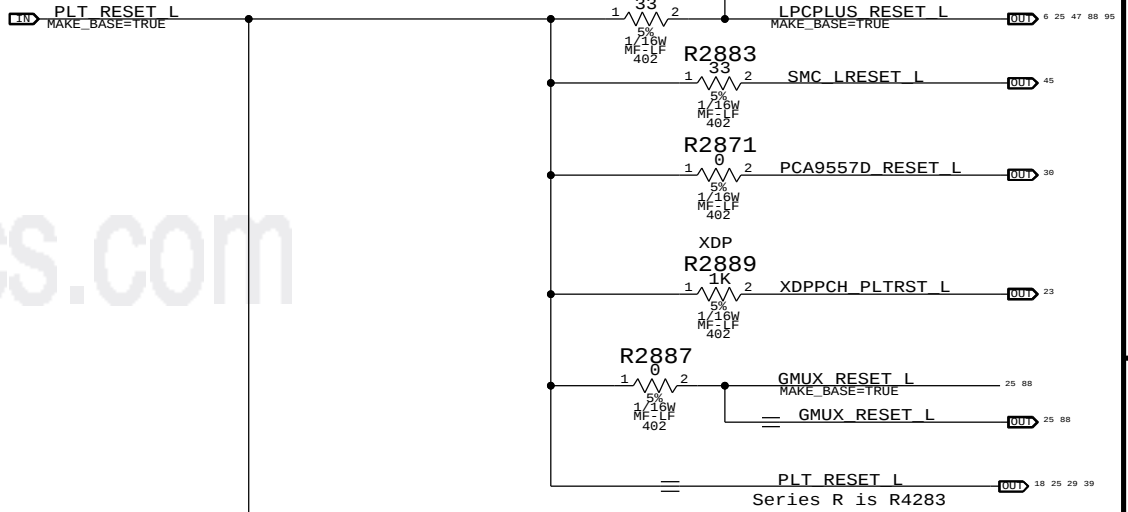


Ethernet WAKE# Isolation



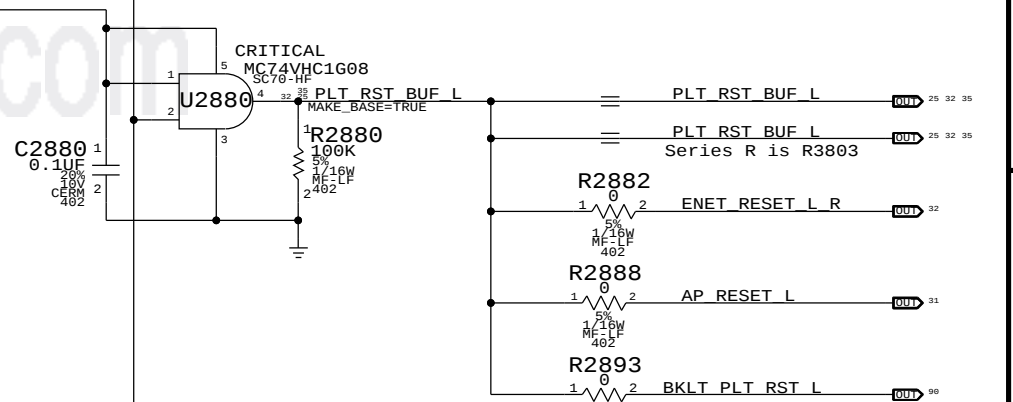
Platform Reset Connections

Unbuffered

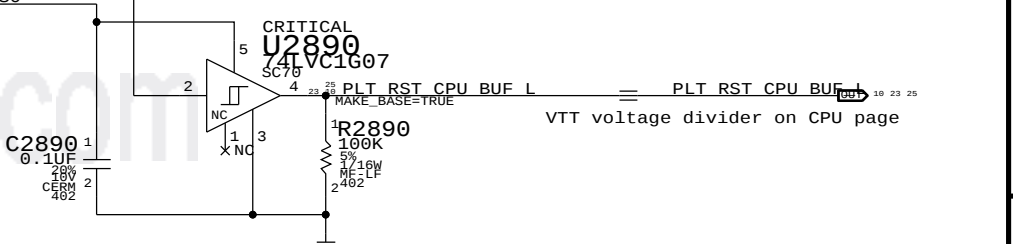


Buffered

Note: Based on K91/K92 layout, ENET, AP and BKLT are moved to Buffered reset.

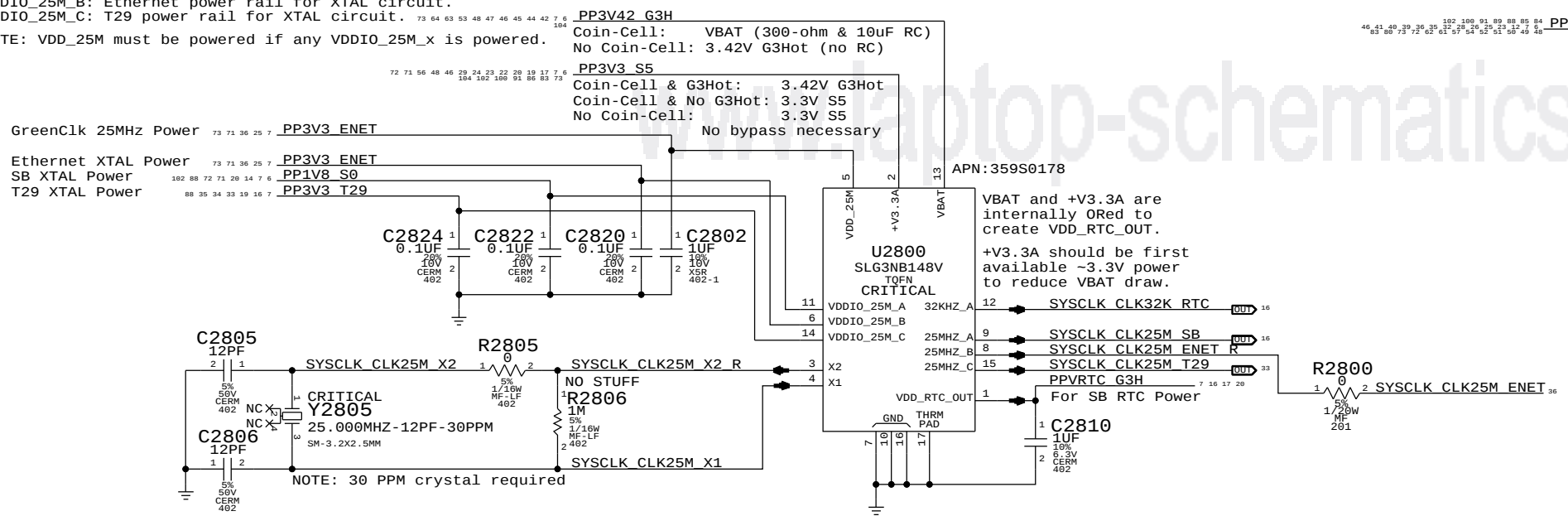


Buffered CPU reset

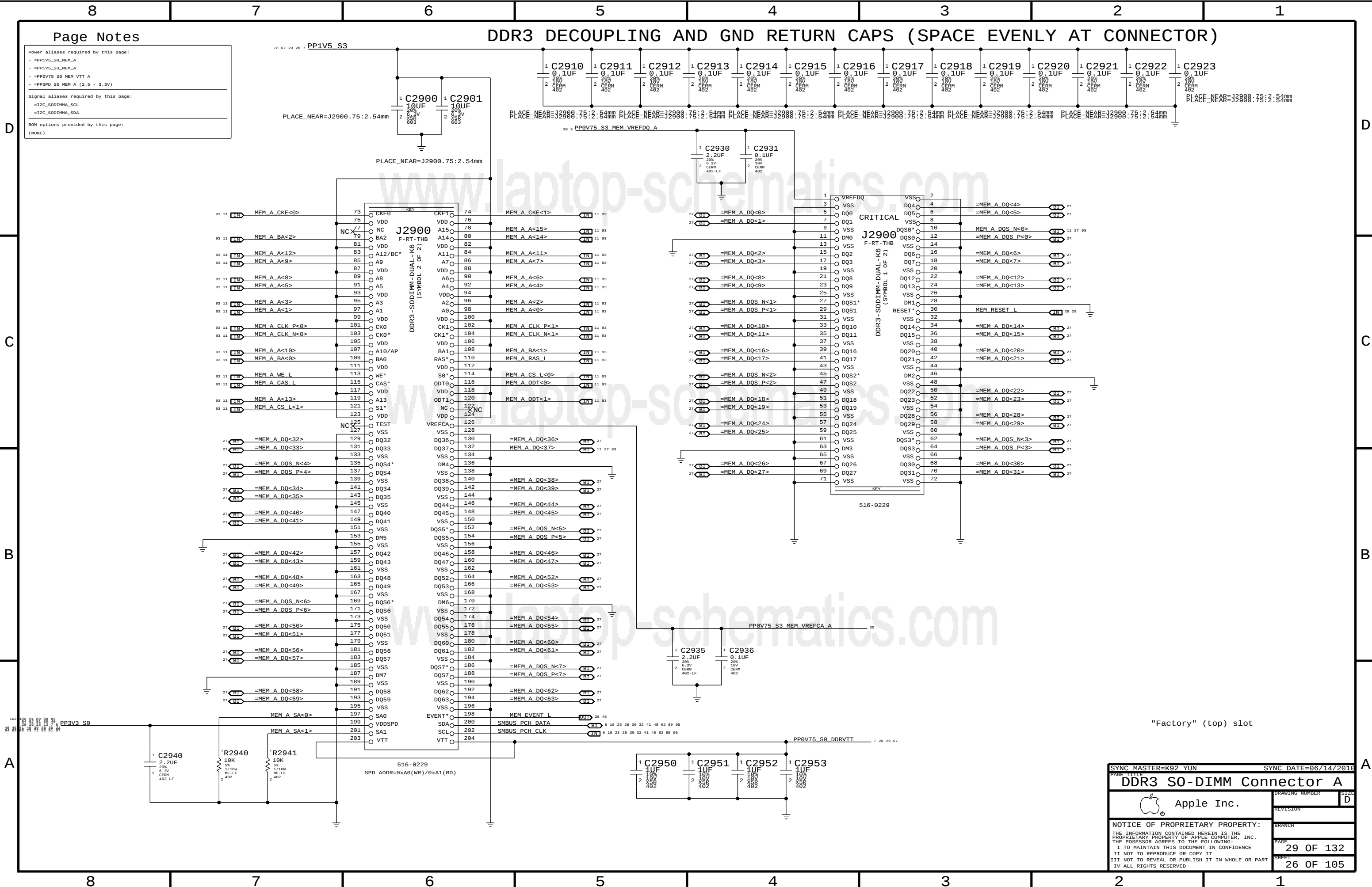


System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.
NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.



SYNC MASTER=K91 MLB		SYNC DATE=06/29/2016	
PAGE TITLE		Chipset Support	
Apple Inc.		DRAWING NUMBER	SIZE D
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		PAGE	28 OF 132
		SHEET	25 OF 105



Page Notes

Power aliases required by this page:

- #PP1V5_S0_MEM_A
- #PP1V5_S3_MEM_A
- #PP0V75_S0_MEM_VTT_A
- #PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- #I2C_SODIMMA_SCL
- #I2C_SODIMMA_SDA

BOM options provided by this page:

(NONE)

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

SYNC MASTER=K92 YUN		SYNC DATE=06/14/2016	
PAGE TITLE			
DDR3 SO-DIMM Connector A			
 Apple Inc.		DRAWING NUMBER	SIZE
		REVISION	D
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8	7	6	5	4	3	2	1
D	CPU CHANNEL A DQS 0 -> DIMM A DQS 0		CPU CHANNEL B DQS 0 -> DIMM B DQS 0				
	93 27 26 11	MEM A DQS N<0>	11 26 27 93 93 28 27 11	MEM B DQS N<0>	11 27 28 93		
	93 11	MEM A DQS P<0>	26	93 28 27 11	MEM B DQS P<0>	11 27 28 93	
		MAKE_BASE=TRUE		MAKE_BASE=TRUE			
	93 11	MEM A DQ<7>	26	93 11	MEM B DQ<7>	28	
		MAKE_BASE=TRUE		MAKE_BASE=TRUE			
	93 11	MEM A DQ<6>	26	93 11	MEM B DQ<6>	28	
		MAKE_BASE=TRUE		MAKE_BASE=TRUE			
	93 11	MEM A DQ<5>	26	93 11	MEM B DQ<5>	28	
		MAKE_BASE=TRUE		MAKE_BASE=TRUE			
C	CPU CHANNEL A DQS 1 -> DIMM A DQS 1		CPU CHANNEL B DQS 1 -> DIMM B DQS 1				
	93 11	MEM A DQS N<1>	26	93 11	MEM B DQS N<1>	28	
	93 11	MEM A DQS P<1>	26	93 11	MEM B DQS P<1>	28	
		MAKE_BASE=TRUE		MAKE_BASE=TRUE			
	93 11	MEM A DQ<15>	26	93 11	MEM B DQ<15>	28	
		MAKE_BASE=TRUE		MAKE_BASE=TRUE			
	93 11	MEM A DQ<14>	26	93 11	MEM B DQ<14>	28	
		MAKE_BASE=TRUE		MAKE_BASE=TRUE			
	93 11	MEM A DQ<13>	26	93 11	MEM B DQ<13>	28	
		MAKE_BASE=TRUE		MAKE_BASE=TRUE			
B	CPU CHANNEL A DQS 2 -> DIMM A DQS 2		CPU CHANNEL B DQS 2 -> DIMM B DQS 2				
	93 11	MEM A DQS N<2>	26	93 11	MEM B DQS N<2>	28	
	93 11	MEM A DQS P<2>	26	93 11	MEM B DQS P<2>	28	
		MAKE_BASE=TRUE		MAKE_BASE=TRUE			
	93 11	MEM A DQ<23>	26	93 11	MEM B DQ<23>	28	
		MAKE_BASE=TRUE		MAKE_BASE=TRUE			
	93 11	MEM A DQ<22>	26	93 11	MEM B DQ<22>	28	
		MAKE_BASE=TRUE		MAKE_BASE=TRUE			
	93 11	MEM A DQ<21>	26	93 11	MEM B DQ<21>	28	
		MAKE_BASE=TRUE		MAKE_BASE=TRUE			
A	CPU CHANNEL A DQS 3 -> DIMM A DQS 3		CPU CHANNEL B DQS 3 -> DIMM B DQS 3				
	93 11	MEM A DQS N<3>	26	93 11	MEM B DQS N<3>	28	
	93 11	MEM A DQS P<3>	26	93 11	MEM B DQS P<3>	28	
		MAKE_BASE=TRUE		MAKE_BASE=TRUE			
	93 11	MEM A DQ<31>	26	93 11	MEM B DQ<31>	28	
		MAKE_BASE=TRUE		MAKE_BASE=TRUE			
	93 11	MEM A DQ<30>	26	93 11	MEM B DQ<30>	28	
		MAKE_BASE=TRUE		MAKE_BASE=TRUE			
	93 11	MEM A DQ<29>	26	93 11	MEM B DQ<29>	28	
		MAKE_BASE=TRUE		MAKE_BASE=TRUE			

SYNC MASTER=K92 YUN		SYNC DATE=05/14/2010	
PAGE TITLE			
DDR3 Byte/Bit Swaps			
 Apple Inc.		DRAWING NUMBER	SIZE
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		PAGE	30 OF 132
		SHEET	27 OF 105

Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_S0DIMM_SCL
- =I2C_S0DIMM_SDA

BOM options provided by this page:

(NONE)

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

72 67 29 26 7 PP1V5_S3

PLACE_NEAR=J3100.75:2.54mm

PLACE_NEAR=J3100.75:2.54mm

PLACE_NEAR=J3100.75:2.54mm

PLACE_NEAR=J3100.75:2.54mm

PLACE_NEAR=J3100.75:2.54mm

PLACE_NEAR=J3100.75:2.54mm

PLACE_NEAR=J3100.75:2.54mm

PLACE_NEAR=J3100.75:2.54mm

PLACE_NEAR=J3100.75:2.54mm

PLACE_NEAR=J3100.75:2.54mm

D

D

C

C

B

B

A

A

8

7

6

5

4

3

2

1

8

7

6

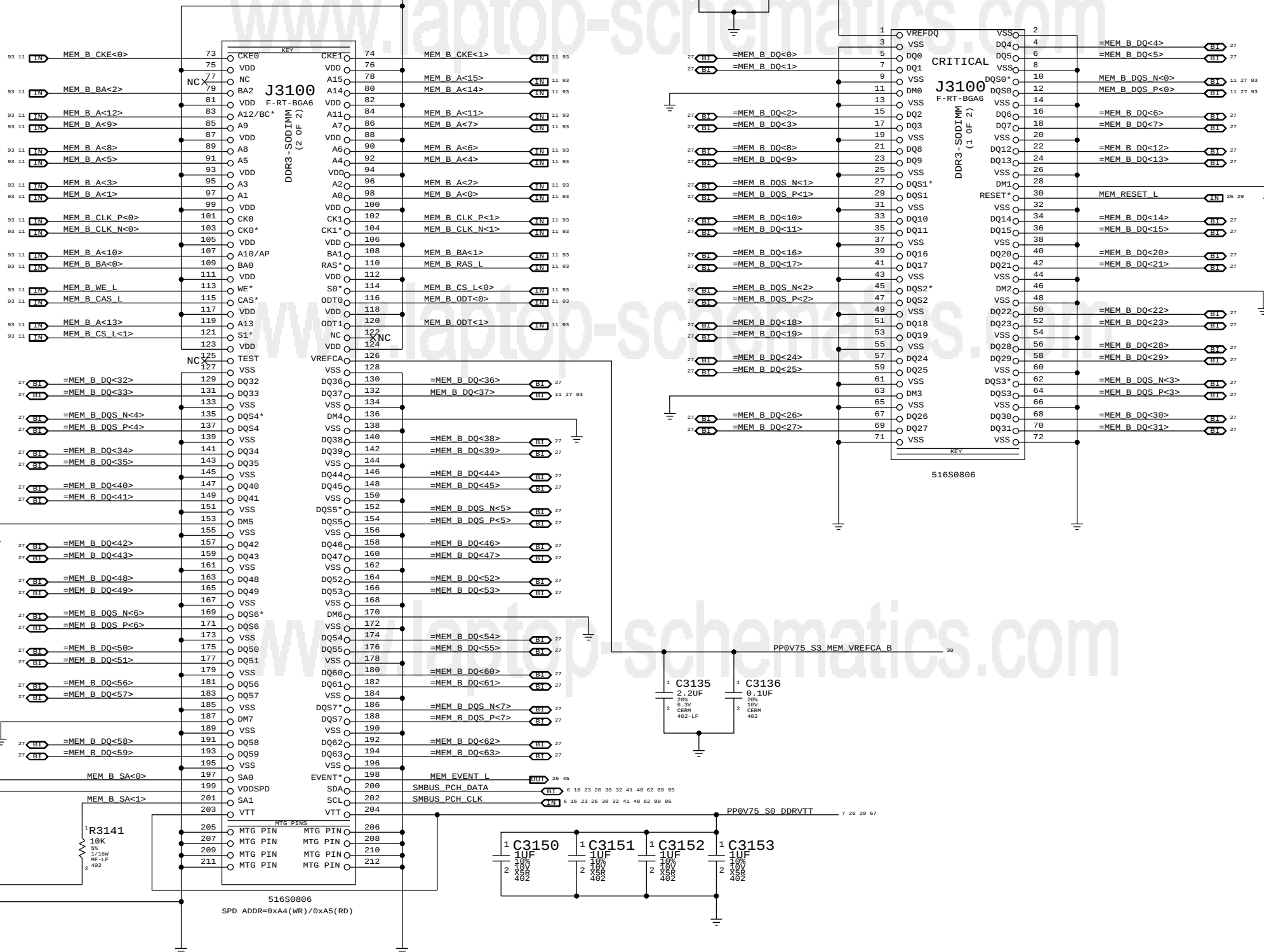
5

4

3

2

1



"Expansion" (bottom) slot

SYNC MASTER=K92_YUN		SYNC DATE=06/14/2016	
DDR3 S0-DIMM Connector B			
Apple Inc.		DRAWING NUMBER	SIZE
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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the S0-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3->S0 transitions determines behavior of signals.

WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

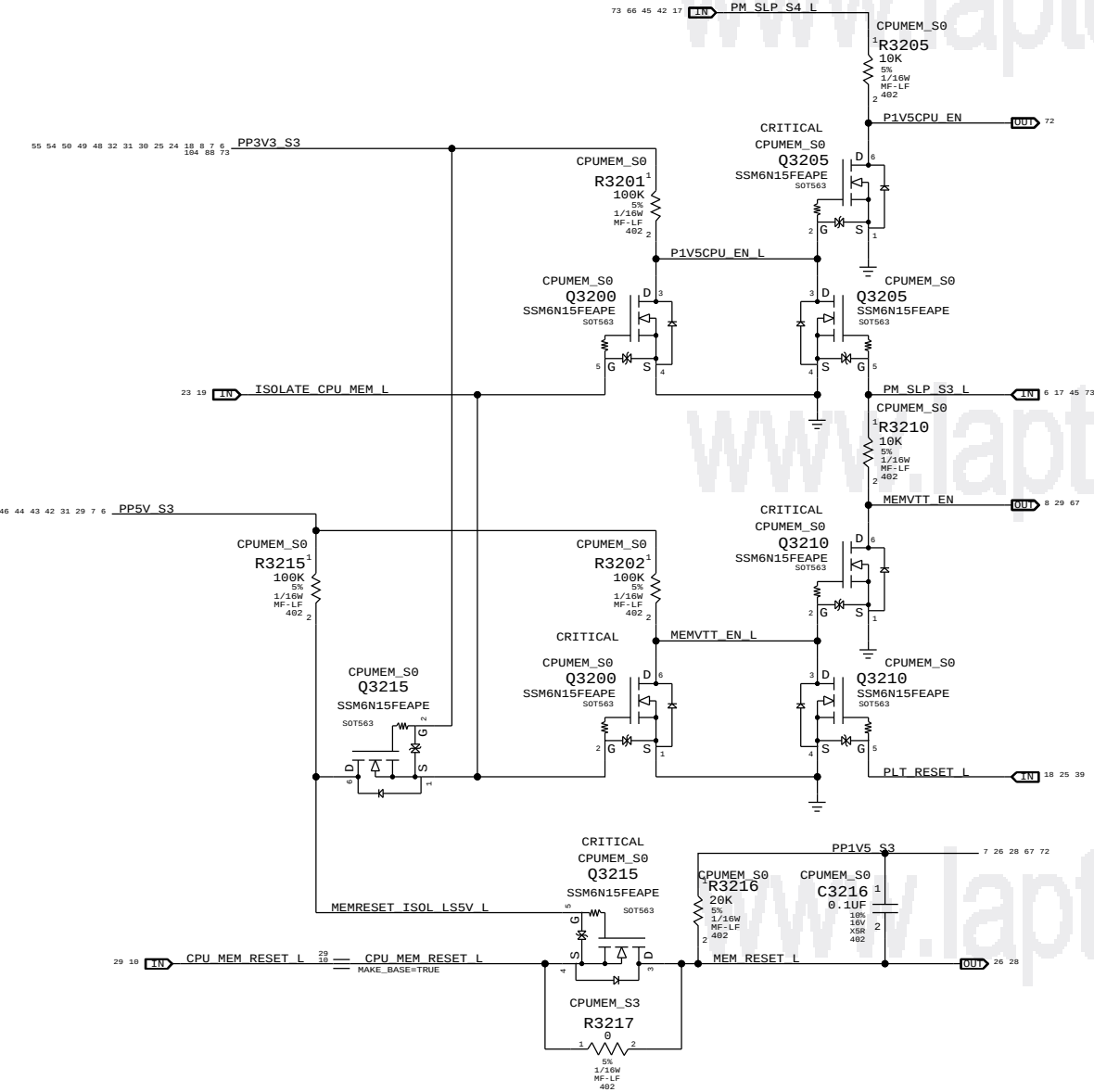
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

$P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L$

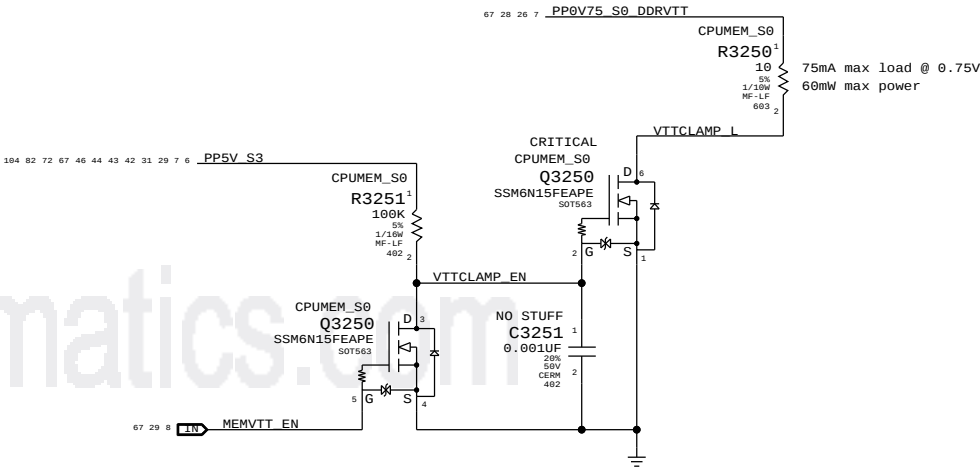
$MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L$

$MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L$

1V5 S0 "PGOOD" for CPU



MEMVTT Clamp
Ensures CKE signals are held low in S3



Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
1	1	0	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC MASTER=K17_MLB

SYNC DATE=04/26/2010

CPU Memory S3 Support

Apple Inc.

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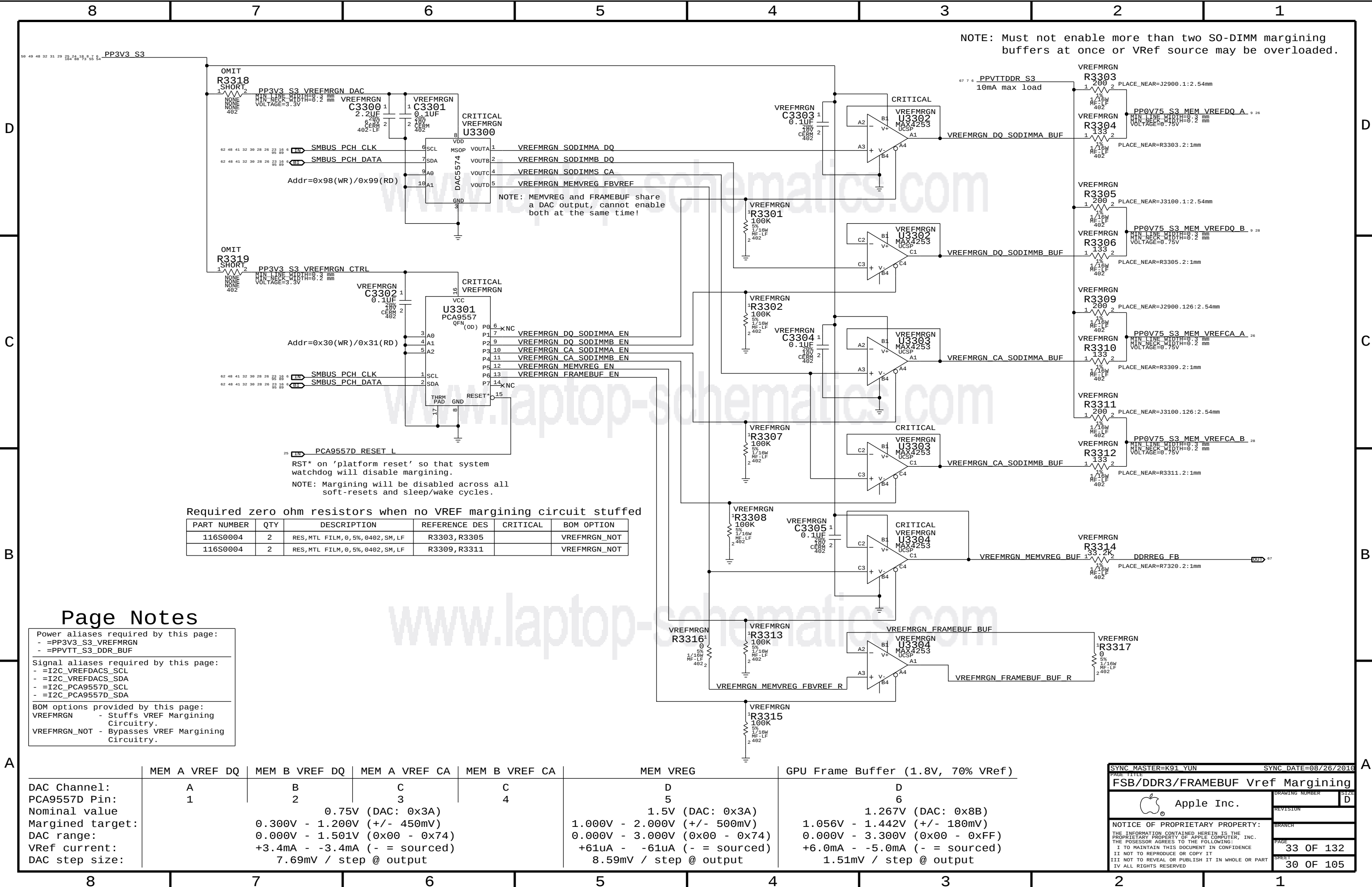
SHEET

SIZE

D

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Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:		+3.4mA - -3.4mA (- = sourced)			+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	1.51mV / step @ output

SYNC MASTER=K91 YUN

SYNC DATE=08/26/2016

PAGE TITLE

FSB/DDR3/FRAMEBUF Vref Margining

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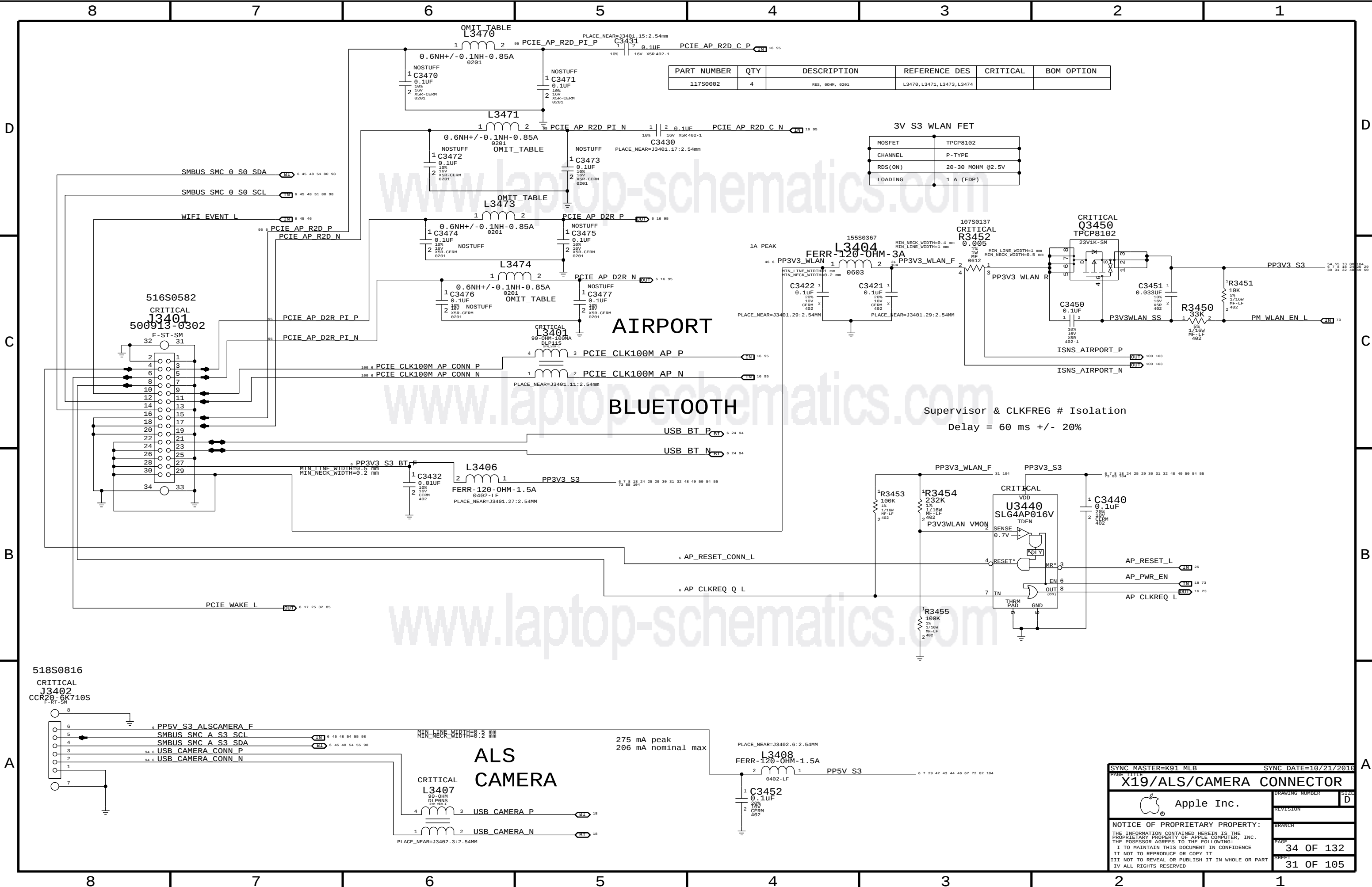
BRANCH

PAGE

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 600M, 0201	L3470, L3471, L3473, L3474		

3V S3 WLAN FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	1 A (EDP)

Supervisor & CLKFREG # Isolation
Delay = 60 ms +/- 20%

SYNC MASTER=K91 MLB

SYNC DATE=10/21/2016

X19/ALS/CAMERA CONNECTOR

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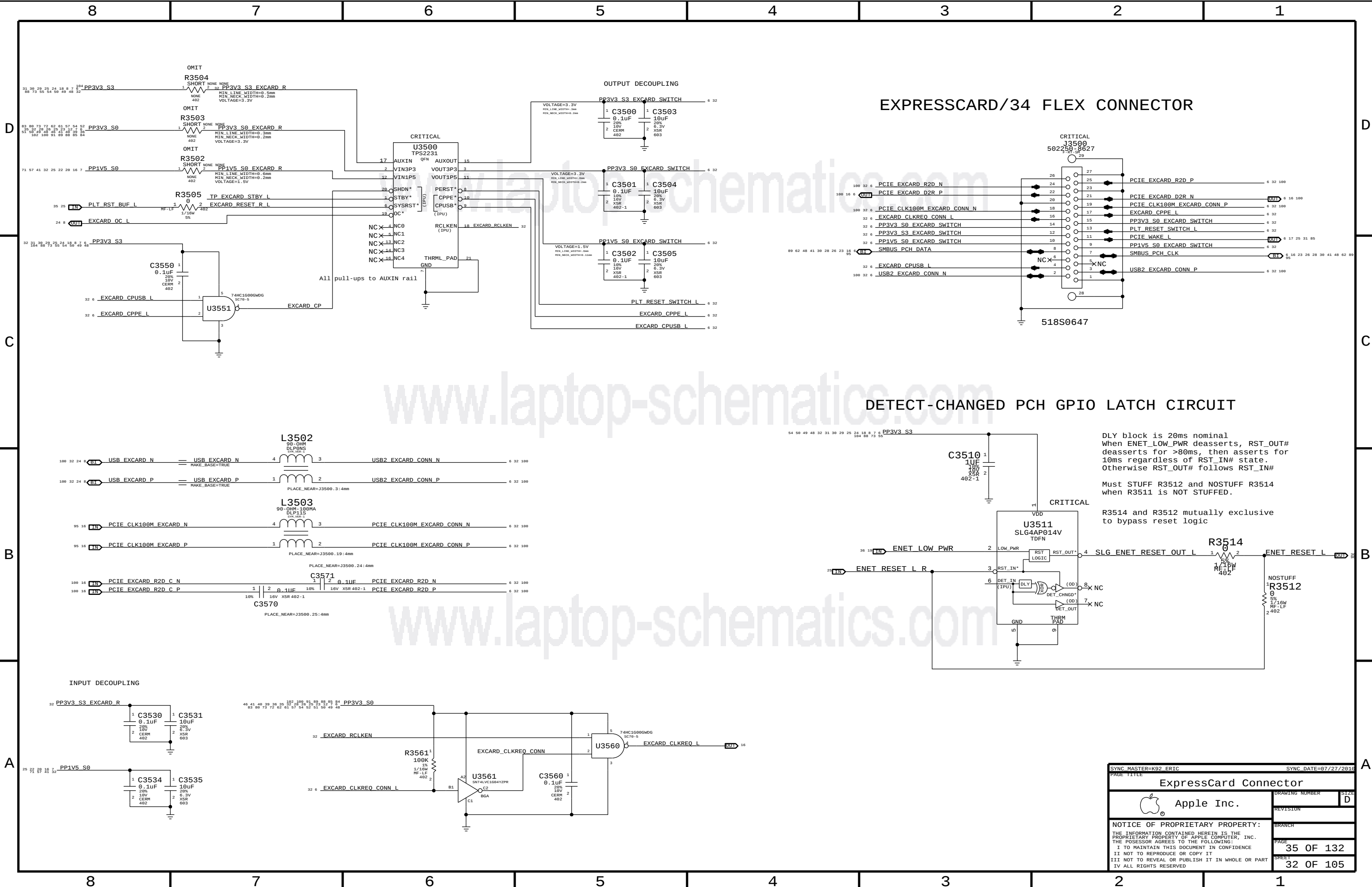
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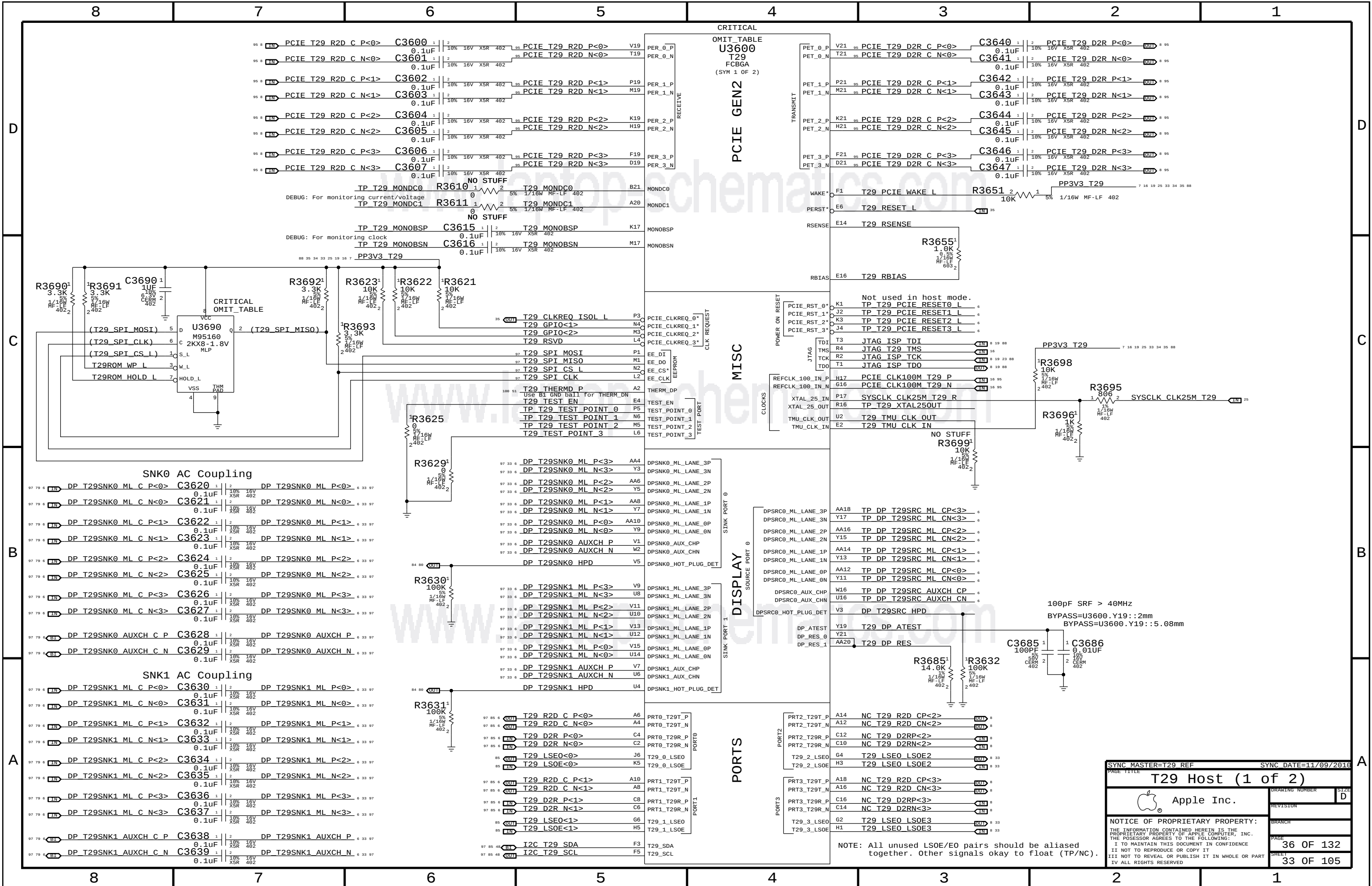
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Page Notes

Power aliases required by this page:

- PPVIN_SW_T29BST (8-13V Boost Input)
- PP18V_T29_REG (18V Boost Output)
- PP3V3_T29_P3V3T29FET (3.3V FET Input)
- PP3V3_T29_FET (3.3V FET Output)
- PP3V3_S0_T29PWRCtrl (1.05V FET Input)
- PP1V05_T29_P1V05T29FET (1.05V FET Output)
- PP1V05_T29_FET (1.05V FET Output)

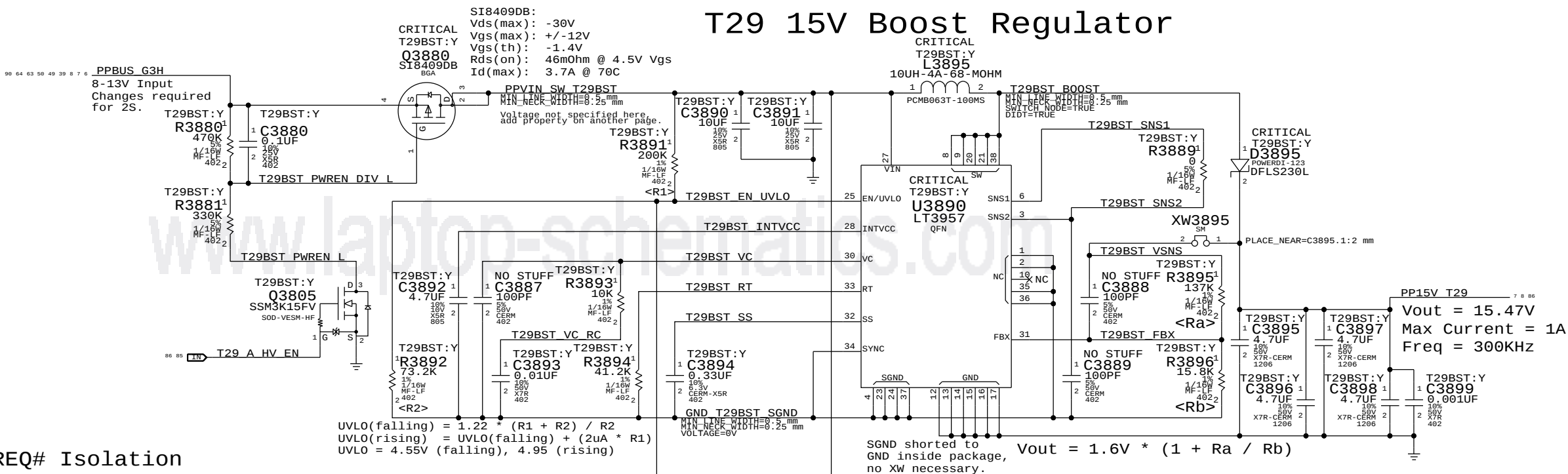
Signal aliases required by this page:

- T29_CLKREQ_L
- T29_RESET_L

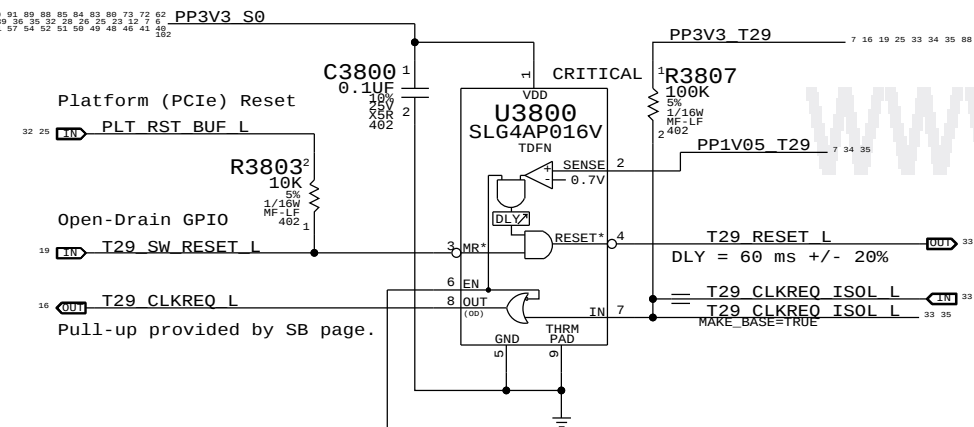
BOM options provided by this page:

T29BST:Y - Stuffs 18V boost circuitry.

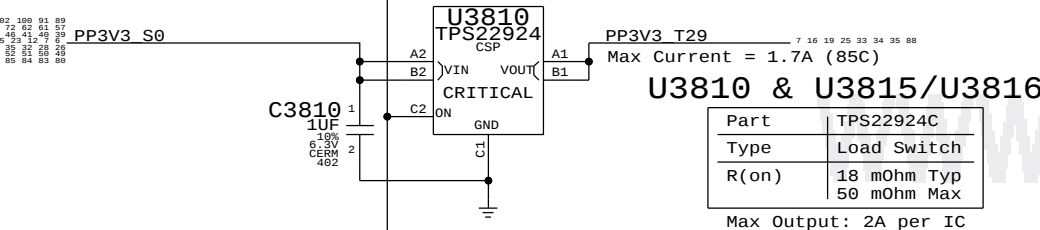
T29 15V Boost Regulator



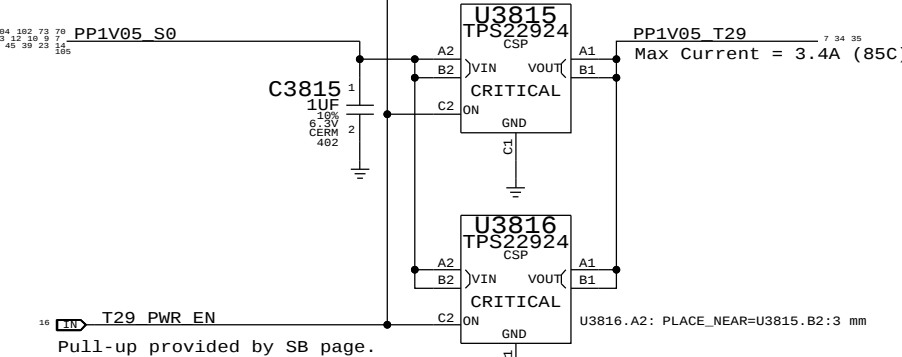
Supervisor & CLKREQ# Isolation



3.3V T29 Switch



1.05V T29 Switch



SYNC MASTER=T29 REF		SYNC DATE=11/09/2016	
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T29 Power Support			
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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

PP3V3_ENET
281mA (1000base-T max power, Caesar IV)

PP1V2_ENET
???mA (1000base-T, Caesar V)

D

D

C

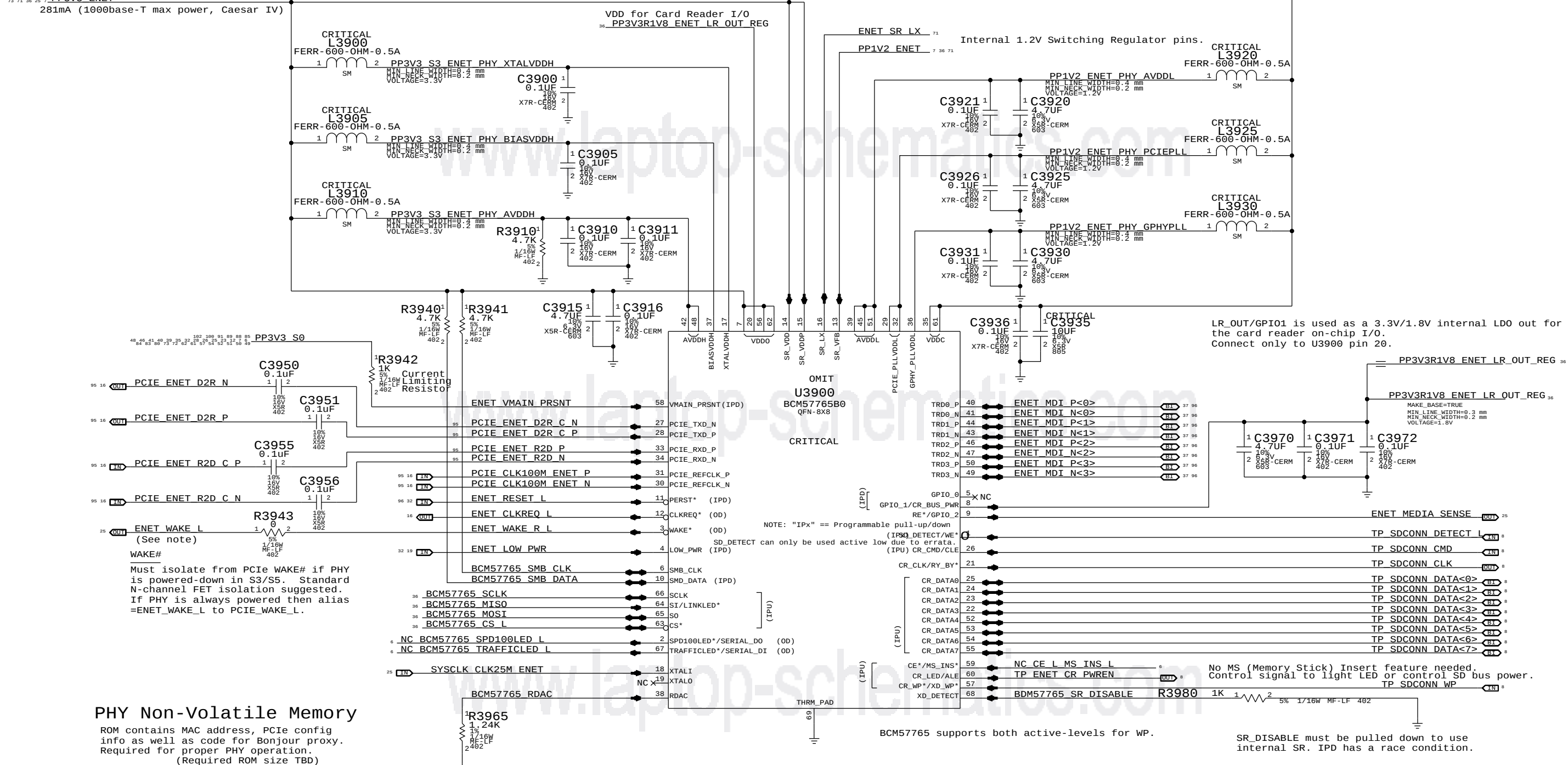
C

B

B

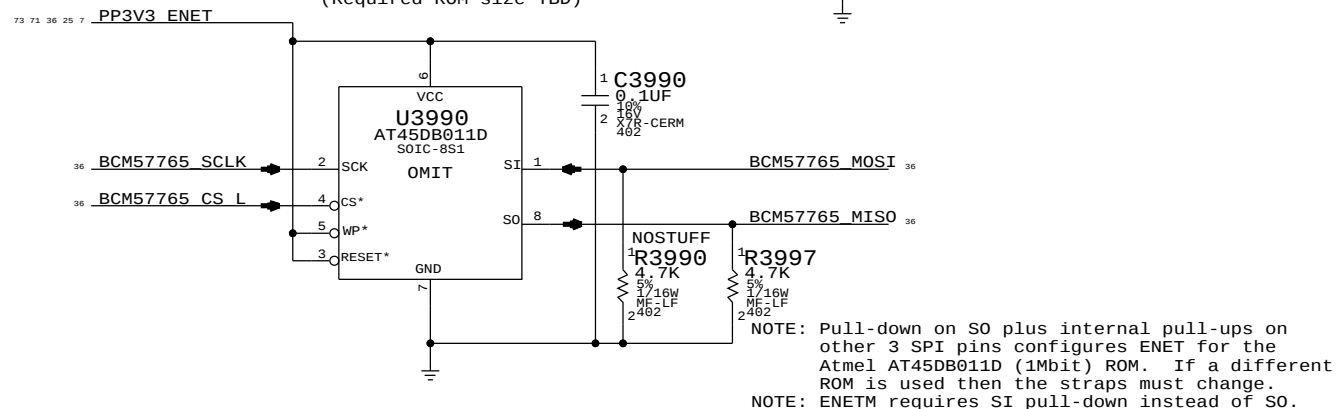
A

A



PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation. (Required ROM size TBD)



BCM57765 supports both active-levels for WP.

SR_DISABLE must be pulled down to use internal SR. IPD has a race condition.

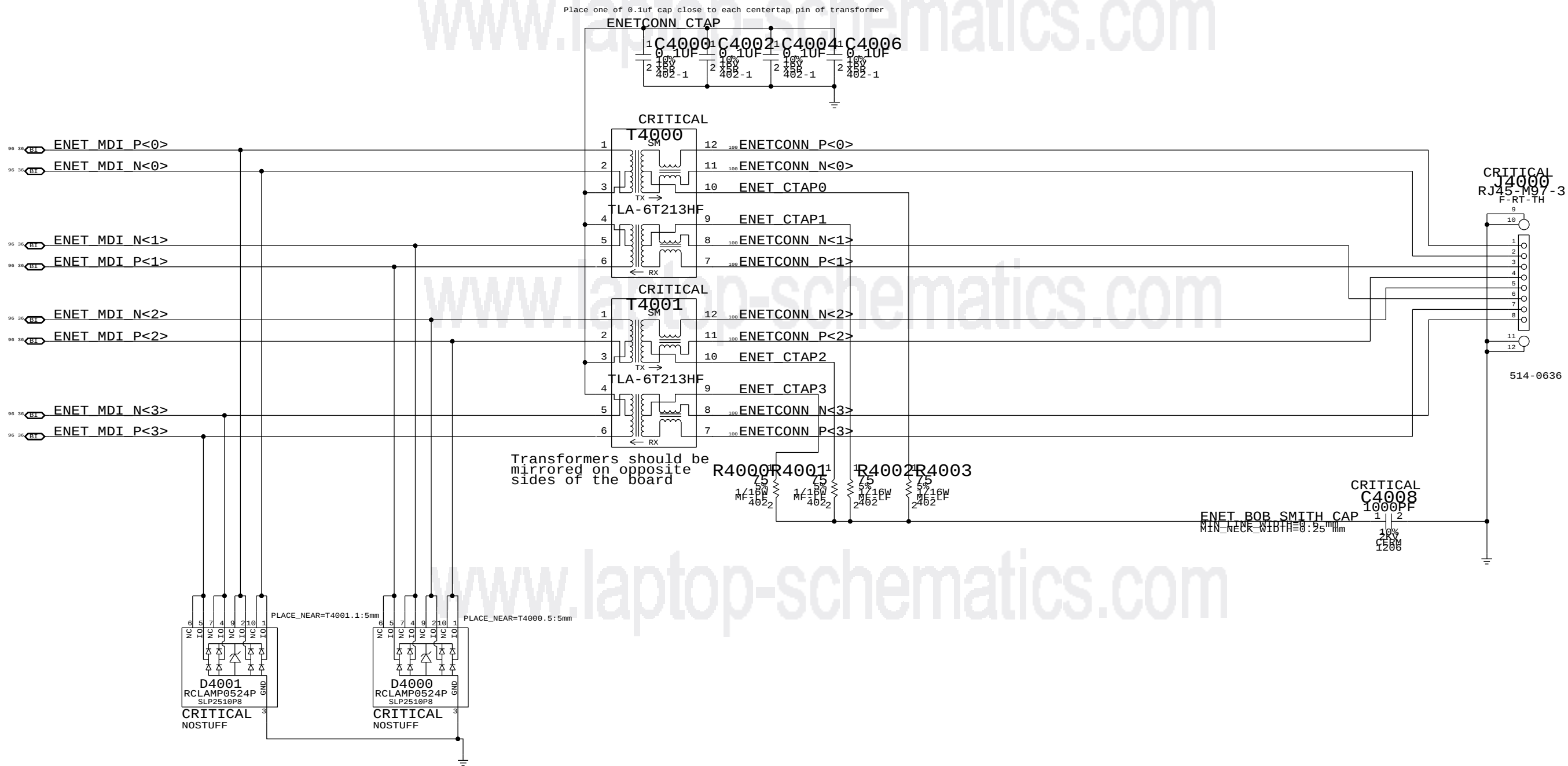
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PAGE 17/17		PAGE 17/17	
ETHERNET PHY (CAESAR IV)		ETHERNET PHY (CAESAR IV)	
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39 OF 132		39 OF 132	
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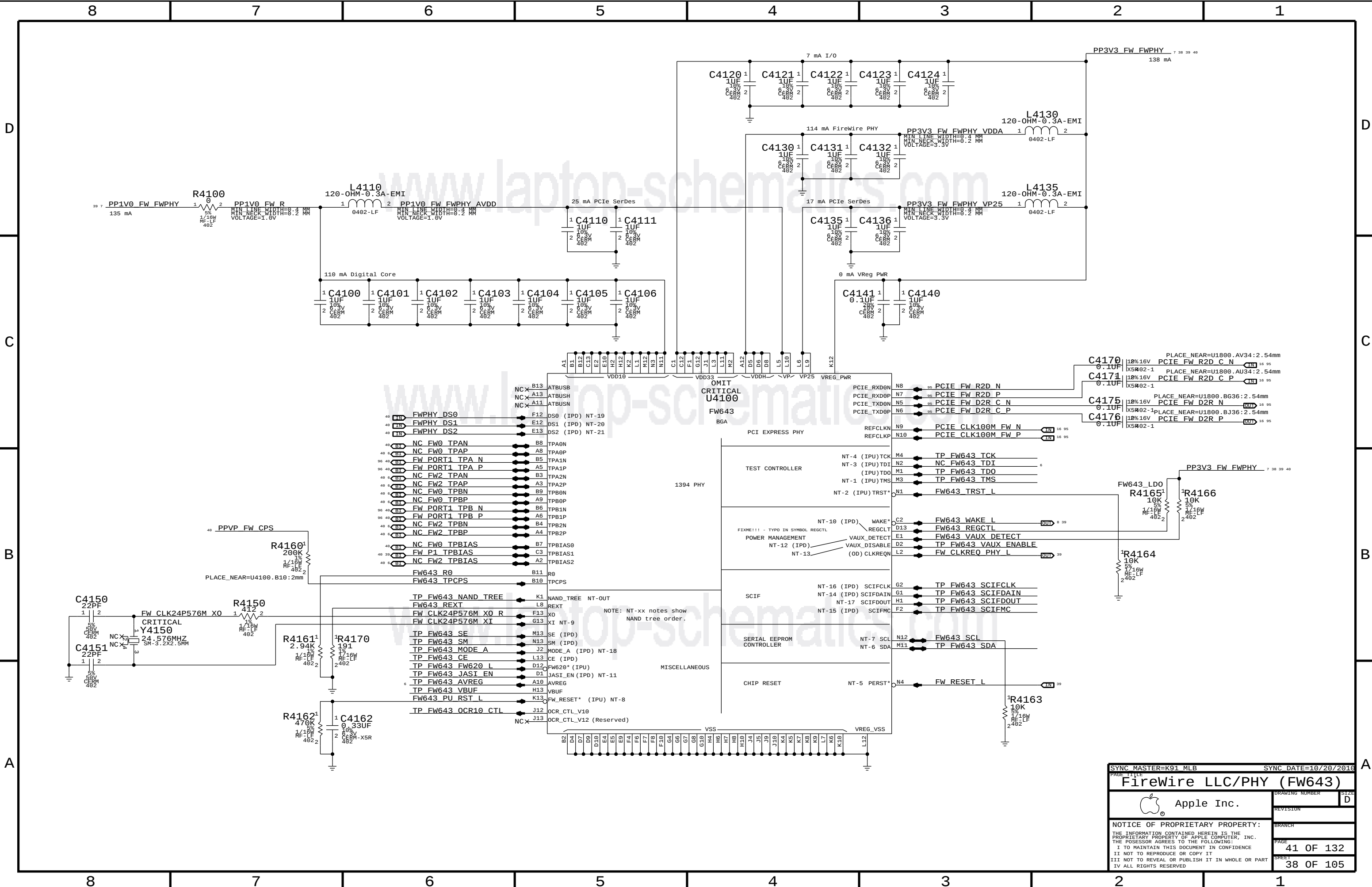
Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC MASTER=K92 ERIC		SYNC DATE=08/24/2016	
PAGE TITLE		Ethernet Connector	
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Page Notes

Power aliases required by this page:

- PPVP_FW_PORT1
- PPVP_FW_PHY_CPS_FET (From Port)
- PPVP_FW_PHY_CPS (To PHY)
- PP3V3_FW_FWPHY
- PP3V3_S0_FWLATEVG

Signal aliases required by this page:

- FW_PHY_DS0
- FW_PHY_DS1
- FW_PHY_DS2

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

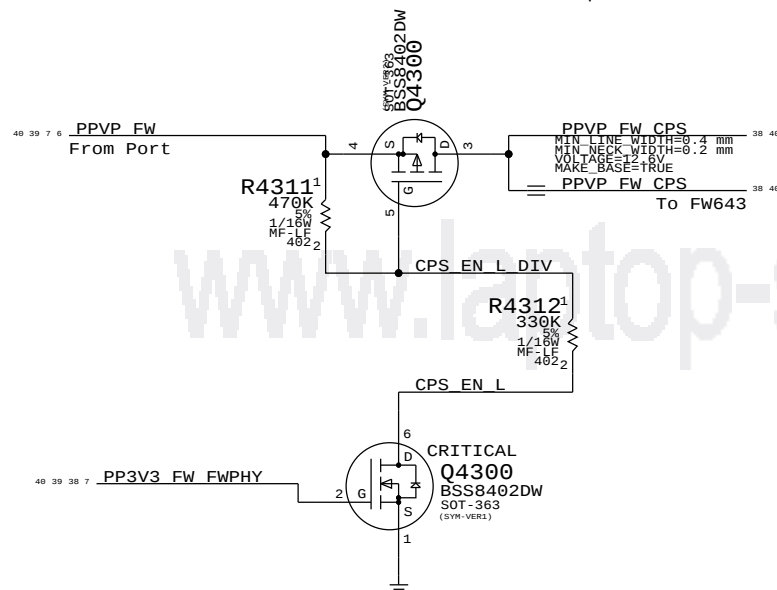
BOM options provided by this page:

(NONE)

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

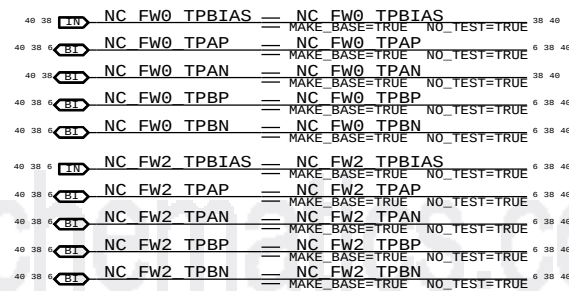
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



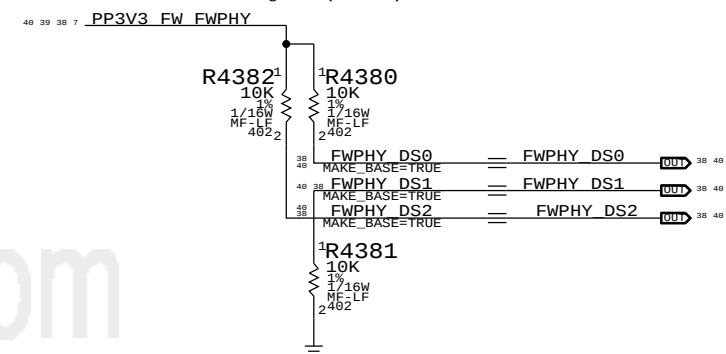
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



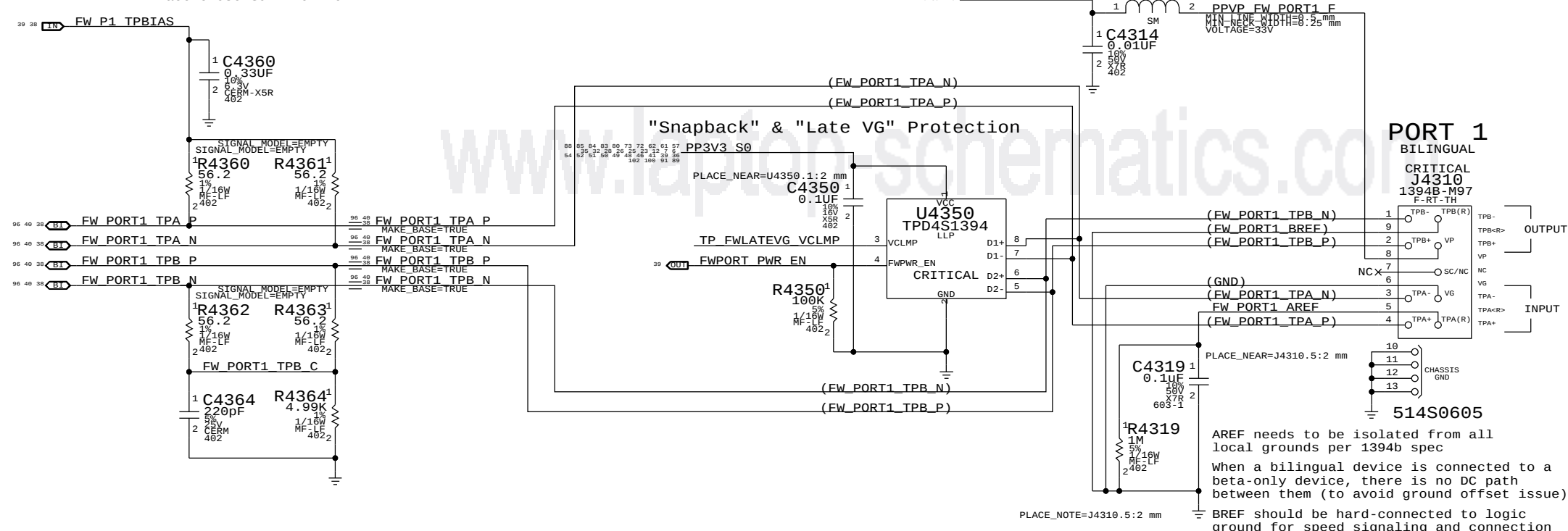
FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)

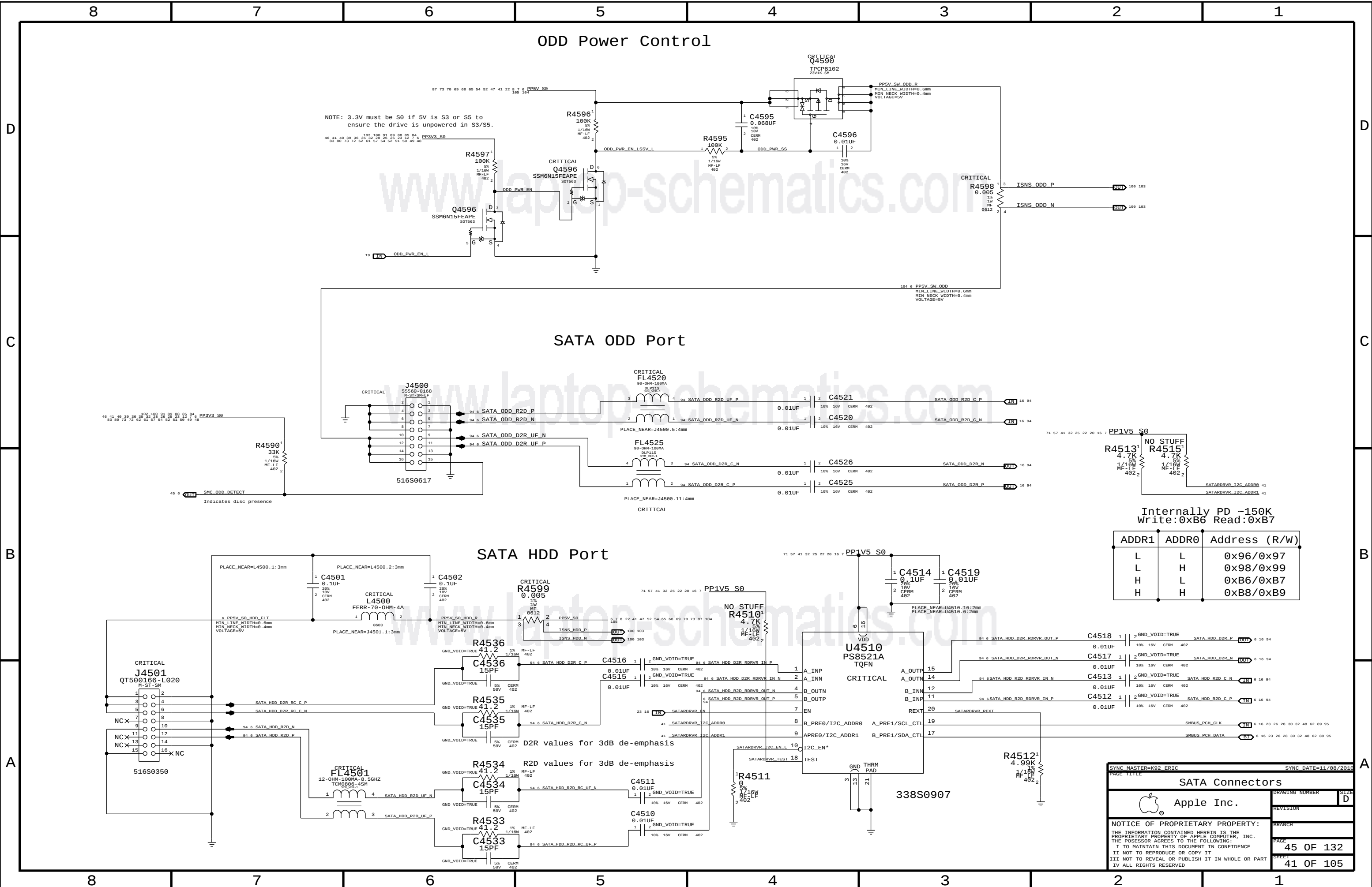


Termination

Place close to FireWire PHY



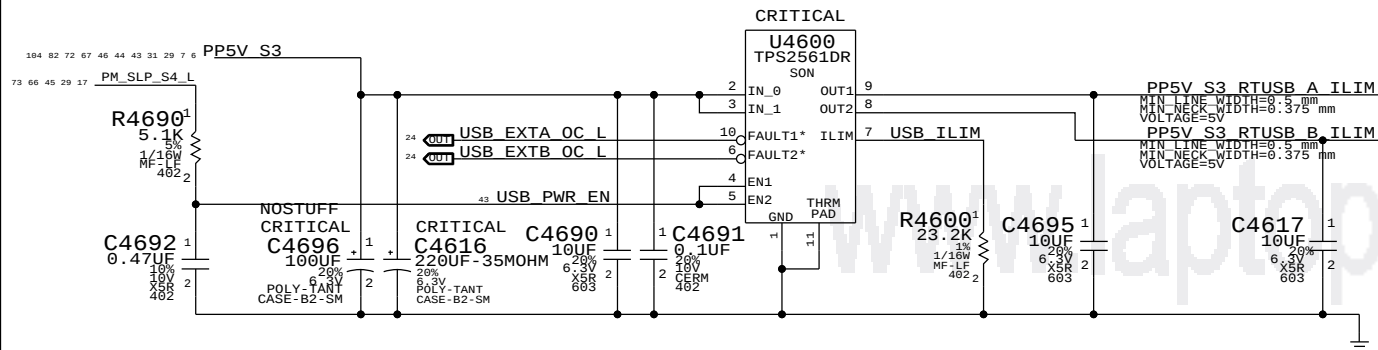
SYNC MASTER=K91 MLB		SYNC DATE=07/22/2016	
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FireWire Connector		SIZE D	
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Internally PD ~150K
Write: 0xB6 Read: 0xB7

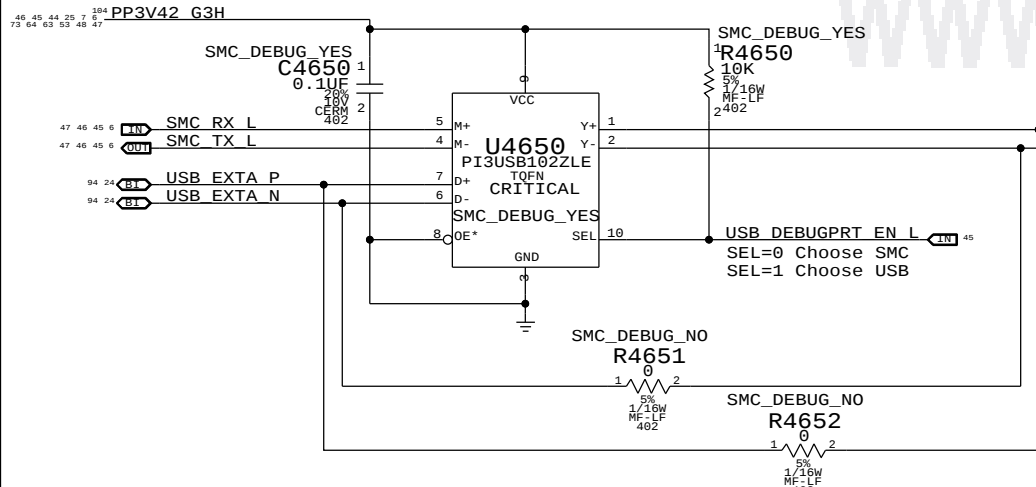
ADDR1	ADDR0	Address (R/W)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9

USB Port Power Switch

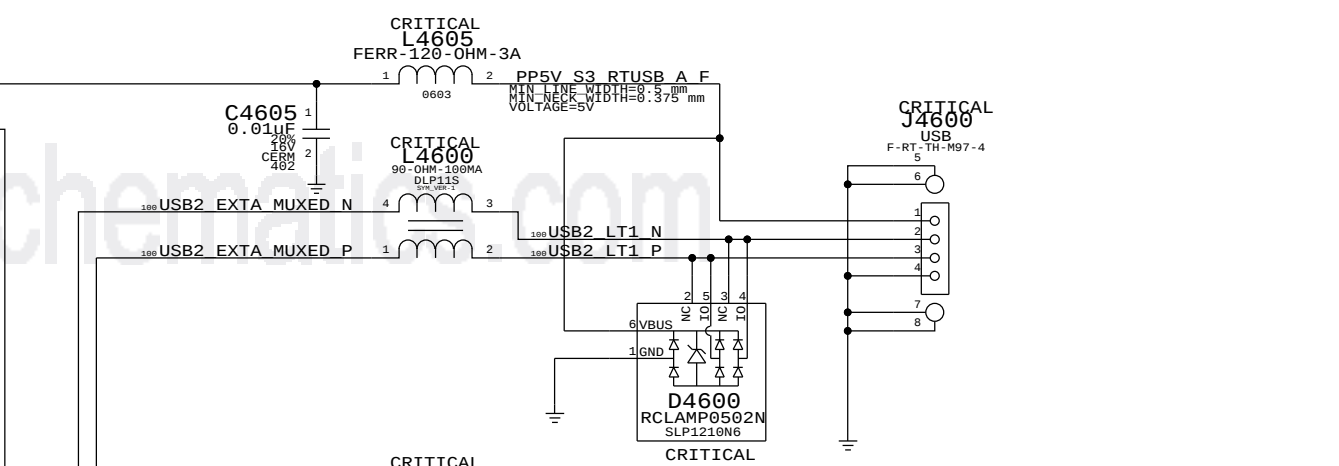


Current limit per port (R4600): 2.18A min / 2.63A max

USB/SMC Debug Mux

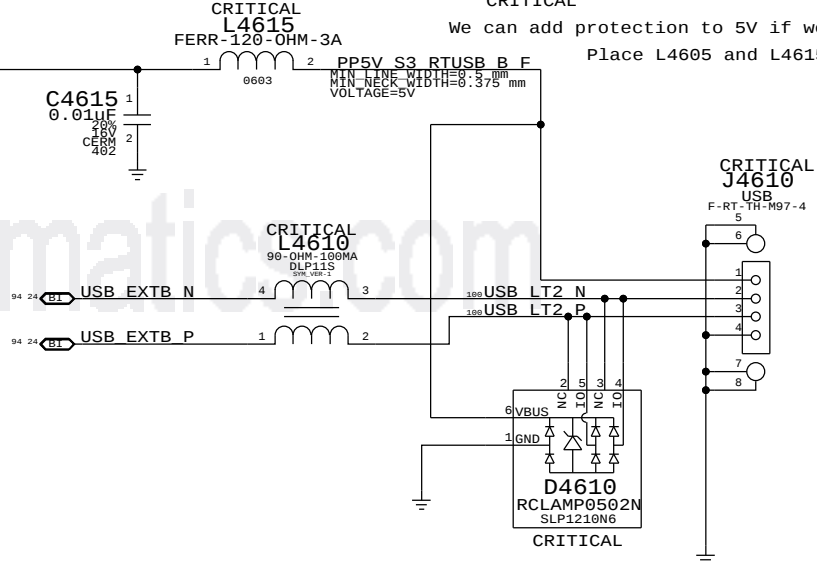


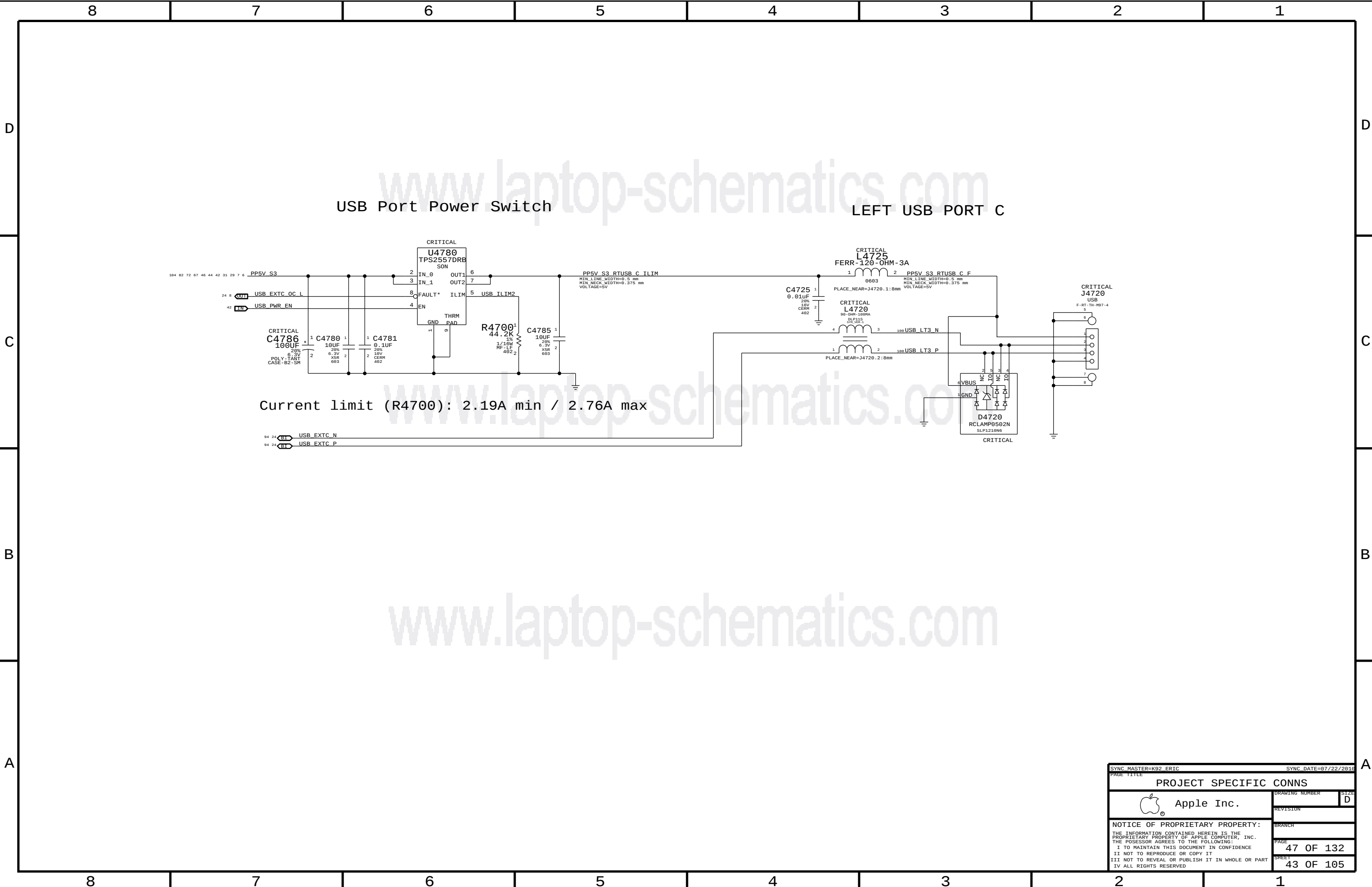
Left USB Port A

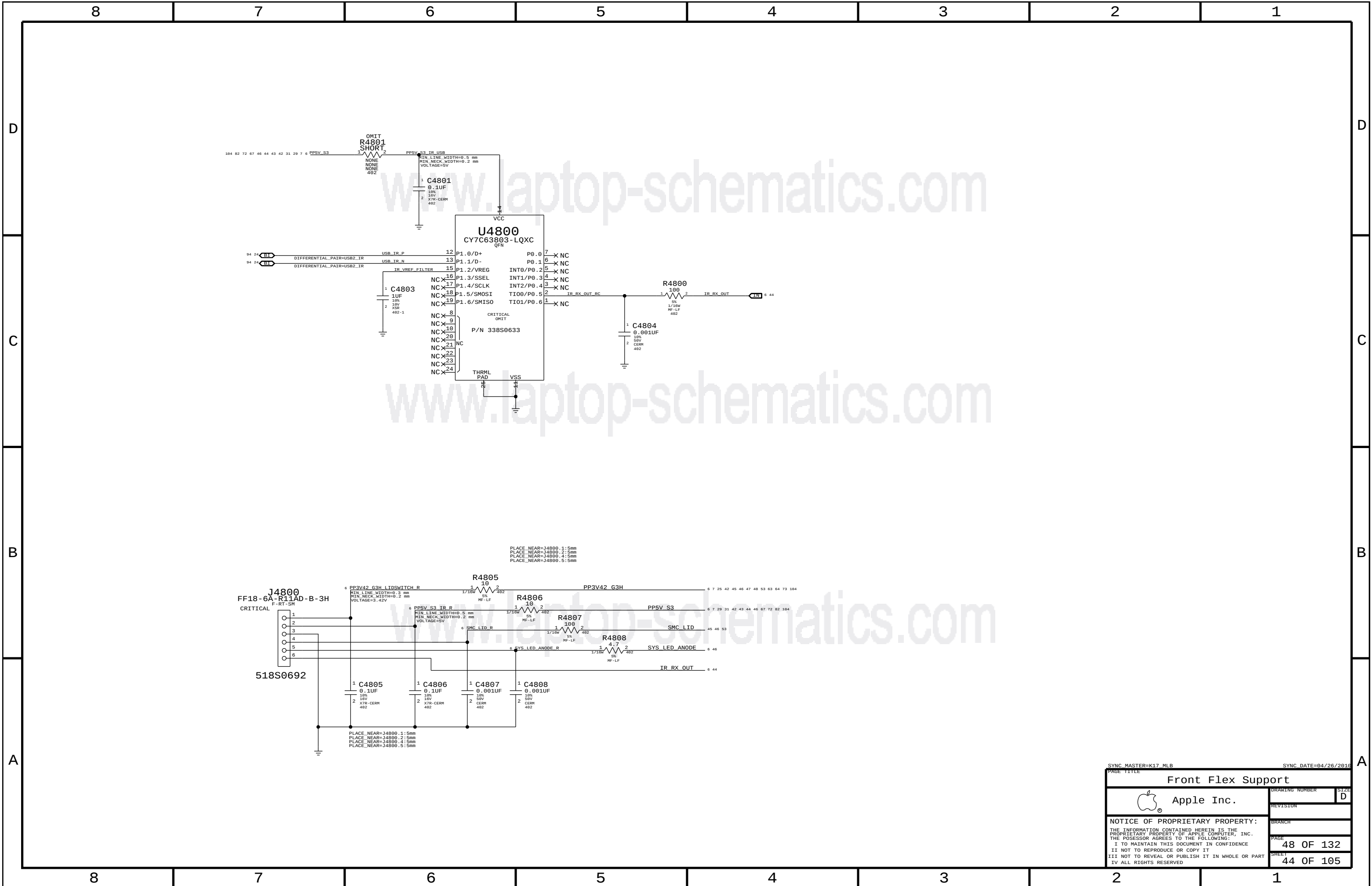


We can add protection to 5V if we want, but leaving NC for now
Place L4605 and L4615 at connector pin

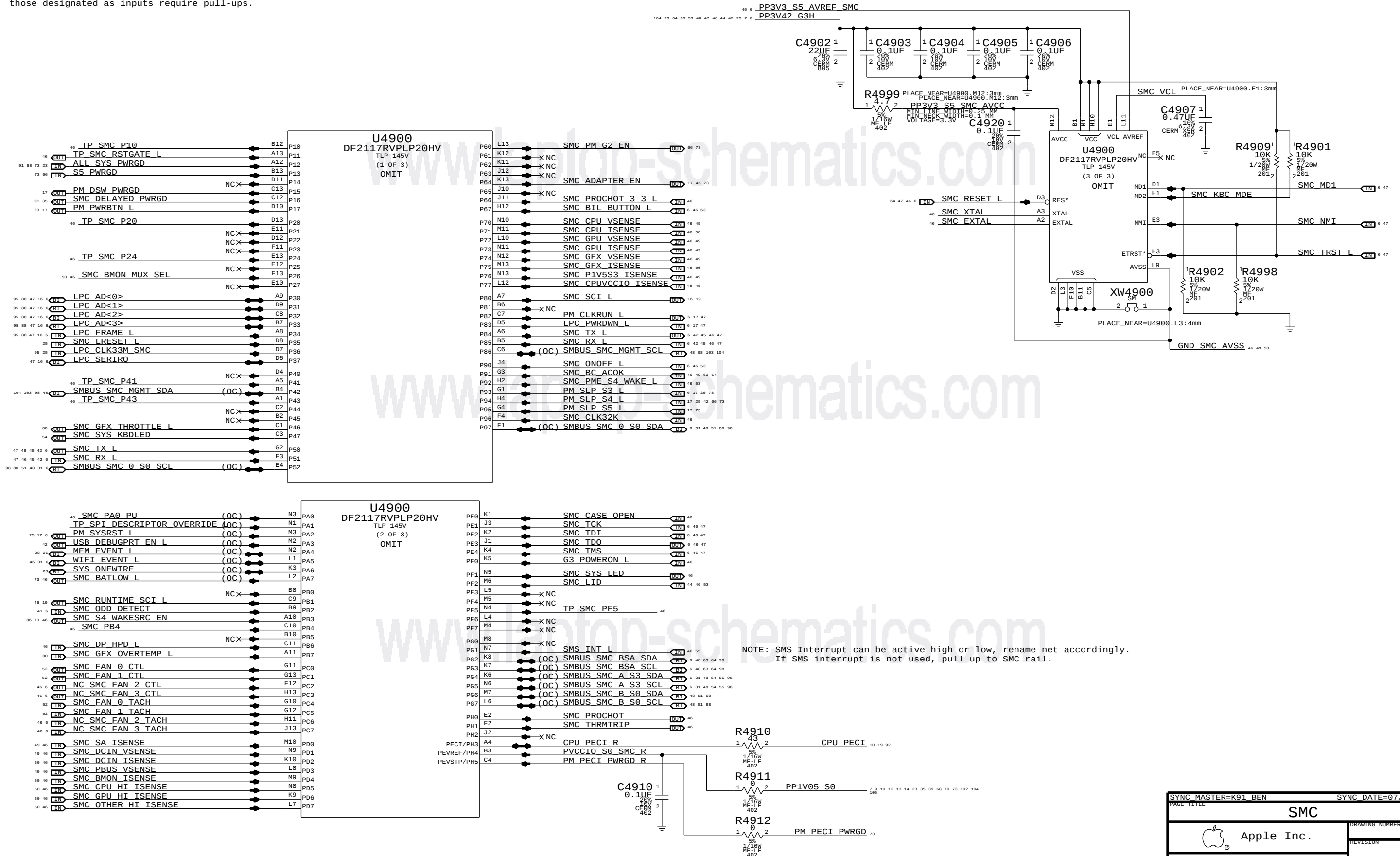
Left USB Port B



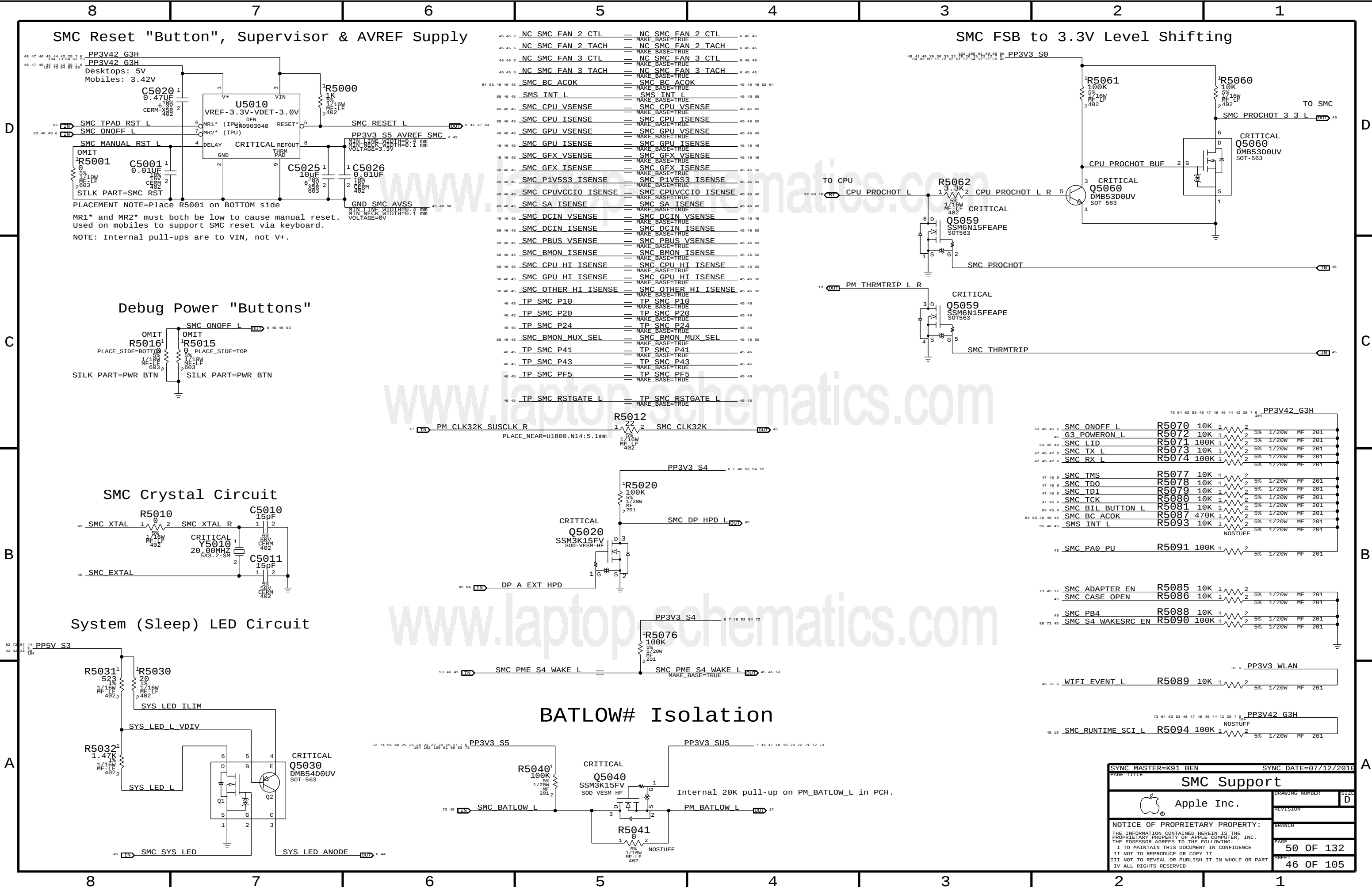


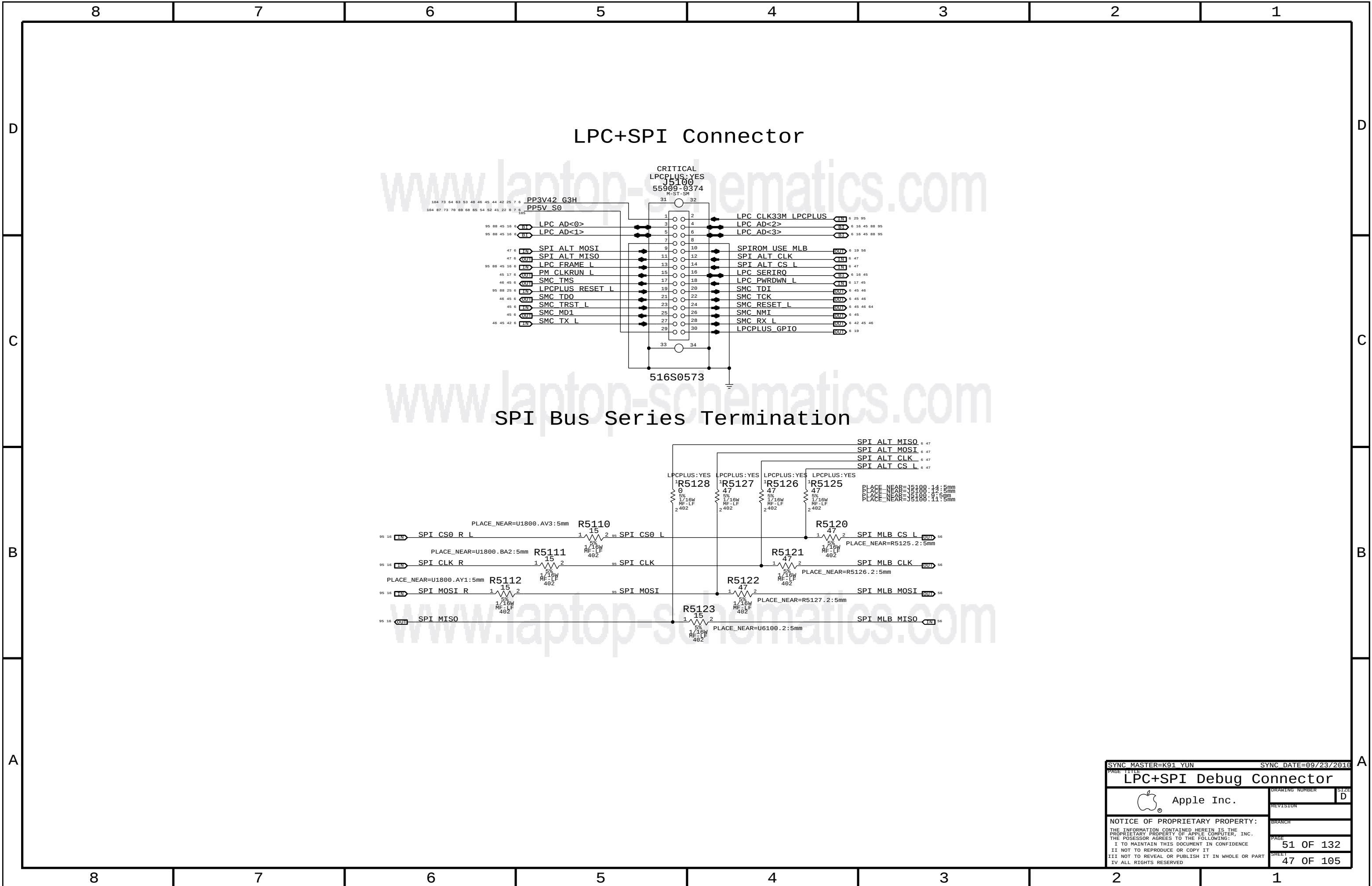


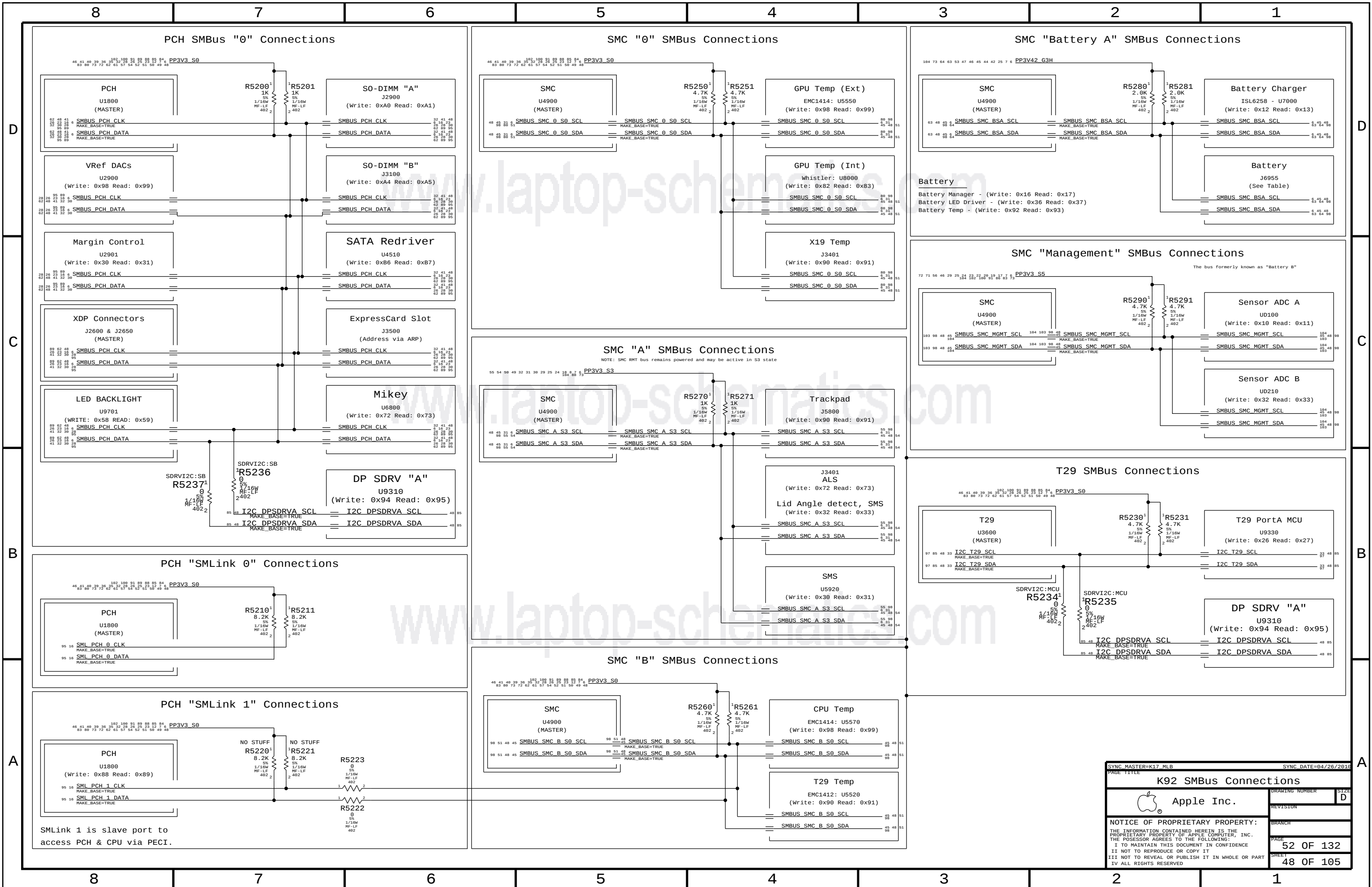
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

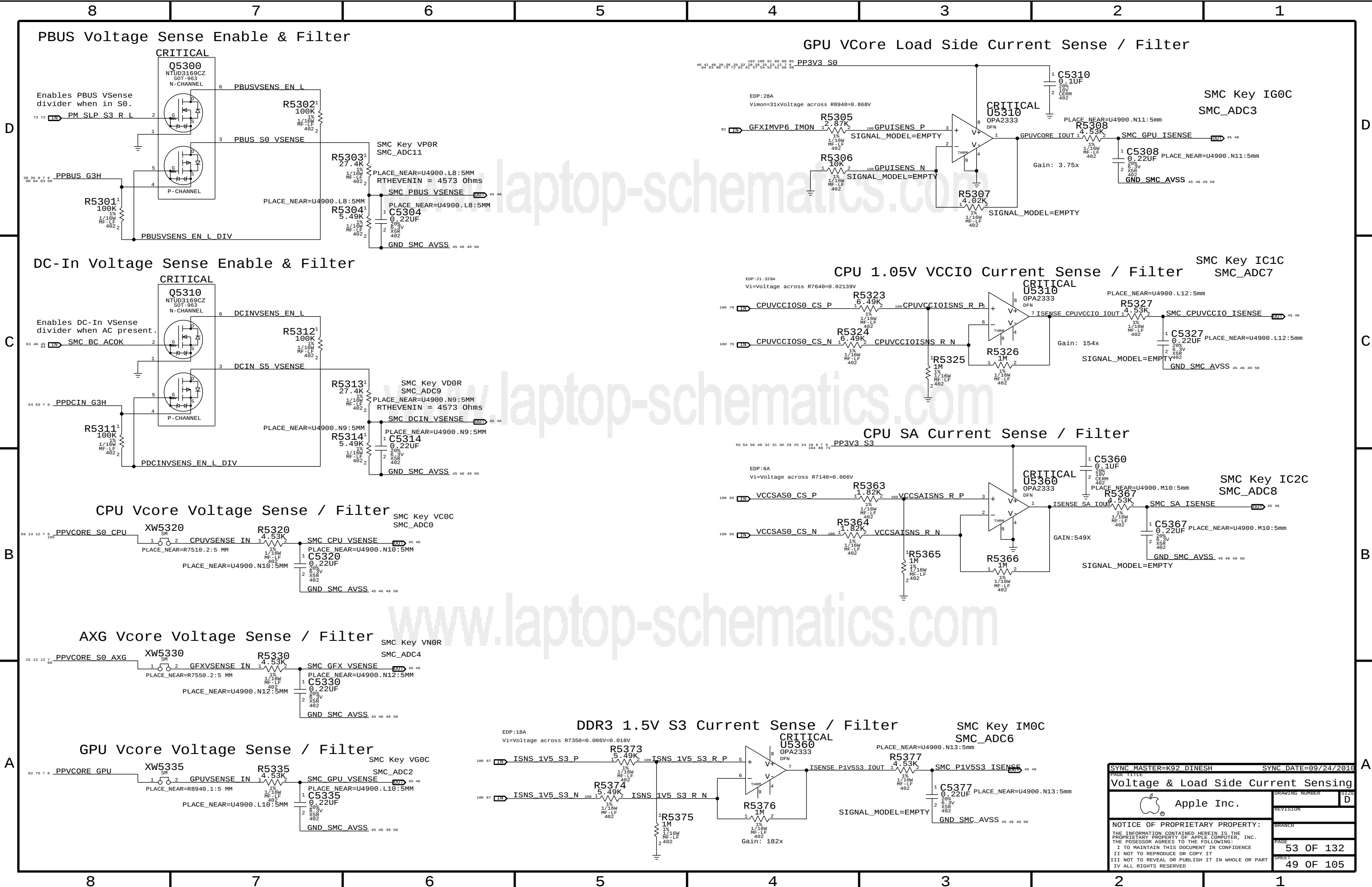


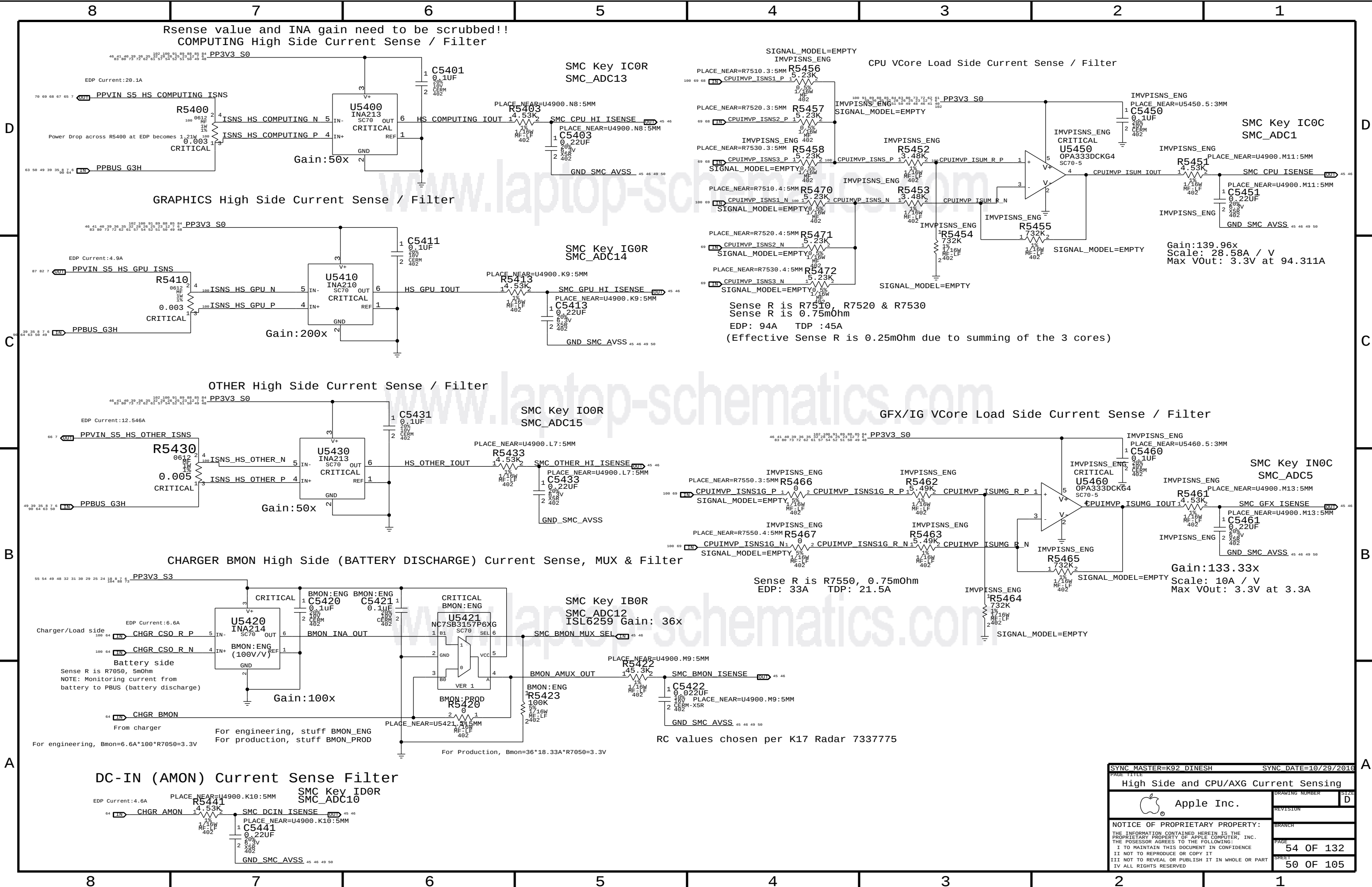
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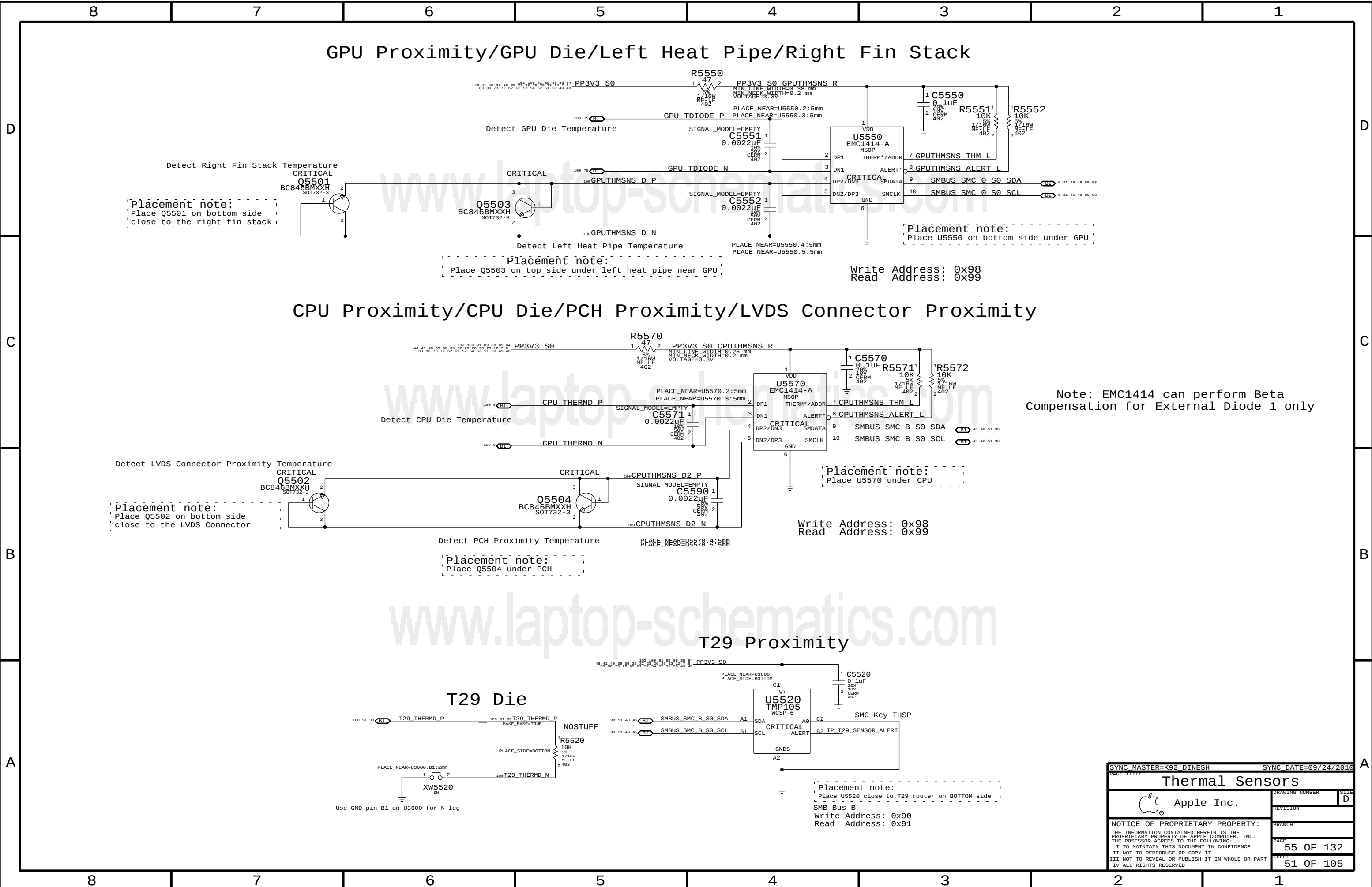












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BOOSTER DESIGN CONSIDERATION:

- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



tect Keyboard backlight, SMC will
 ate and read SMC_SYS_KBDLED:
 w, keyboard backlight present
 GH, keyboard backlight not present
 always stuffed, R5854 only
 ded when KB BL flex connected.

(SMC_KBDLED_PRESENT_L)

CRITICAL

KB BL
J5815

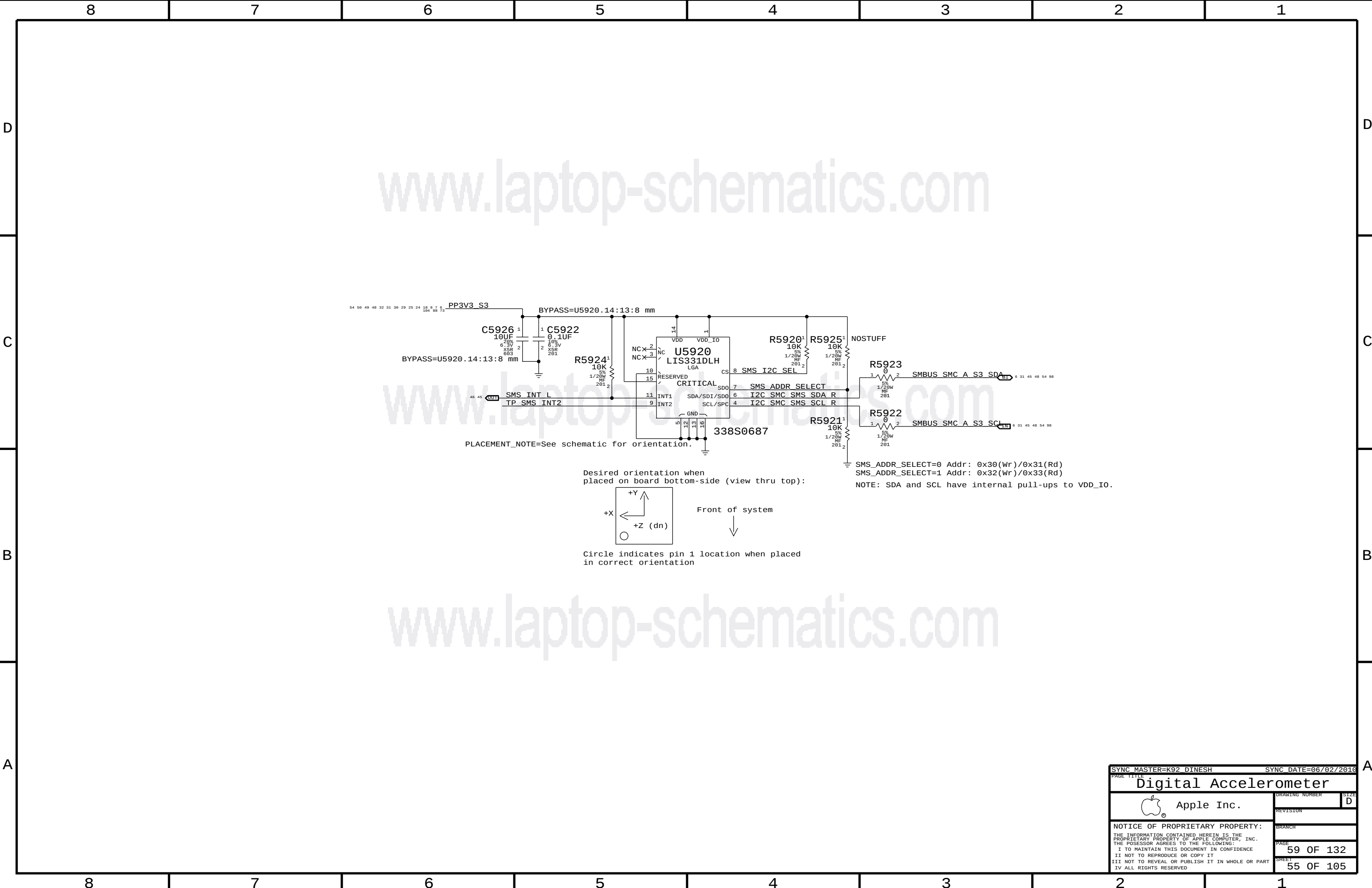
FF18-4A-R11AD-B-3H

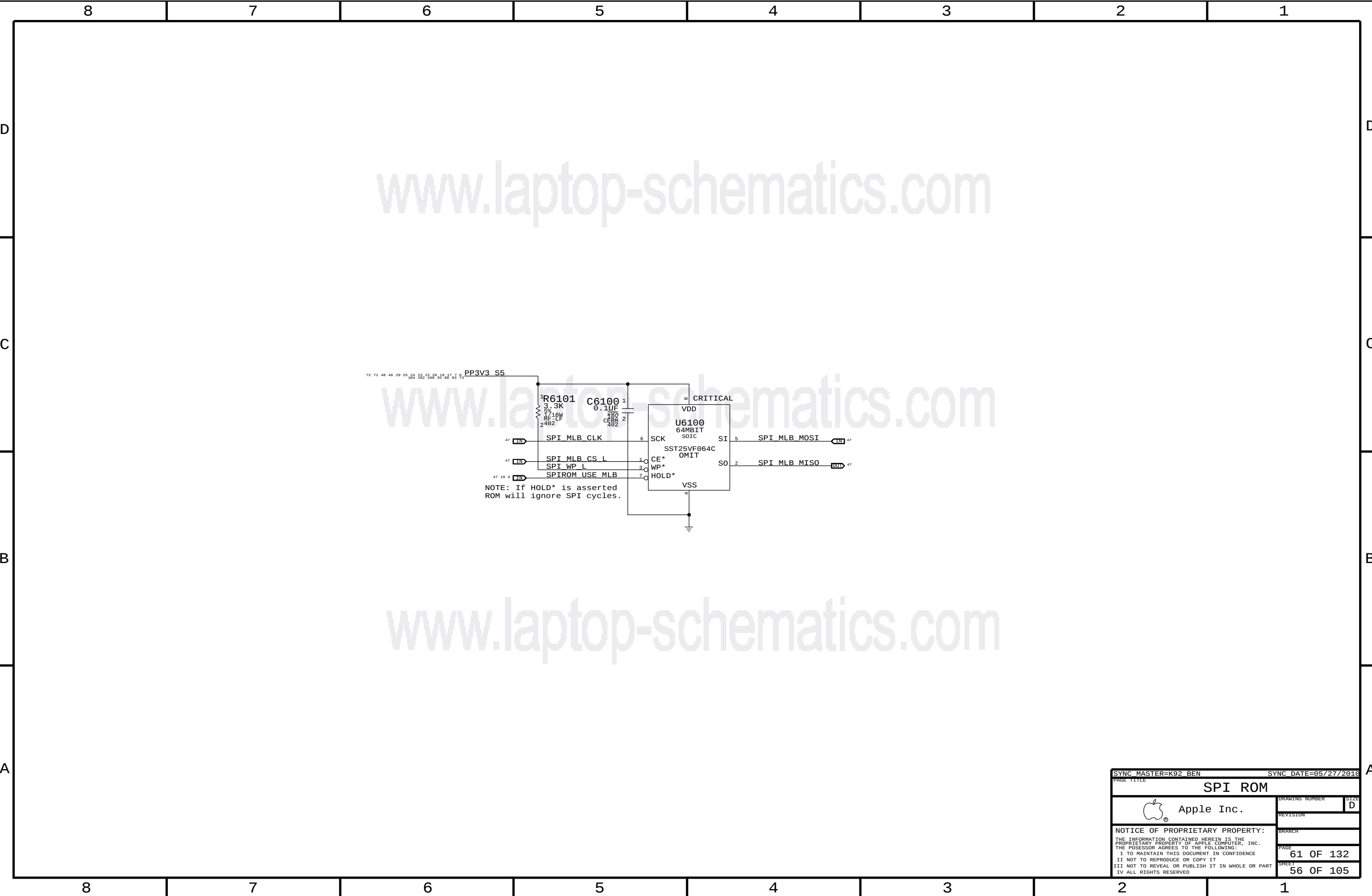
FF18-3H

SMC KDBLED PRESENT L

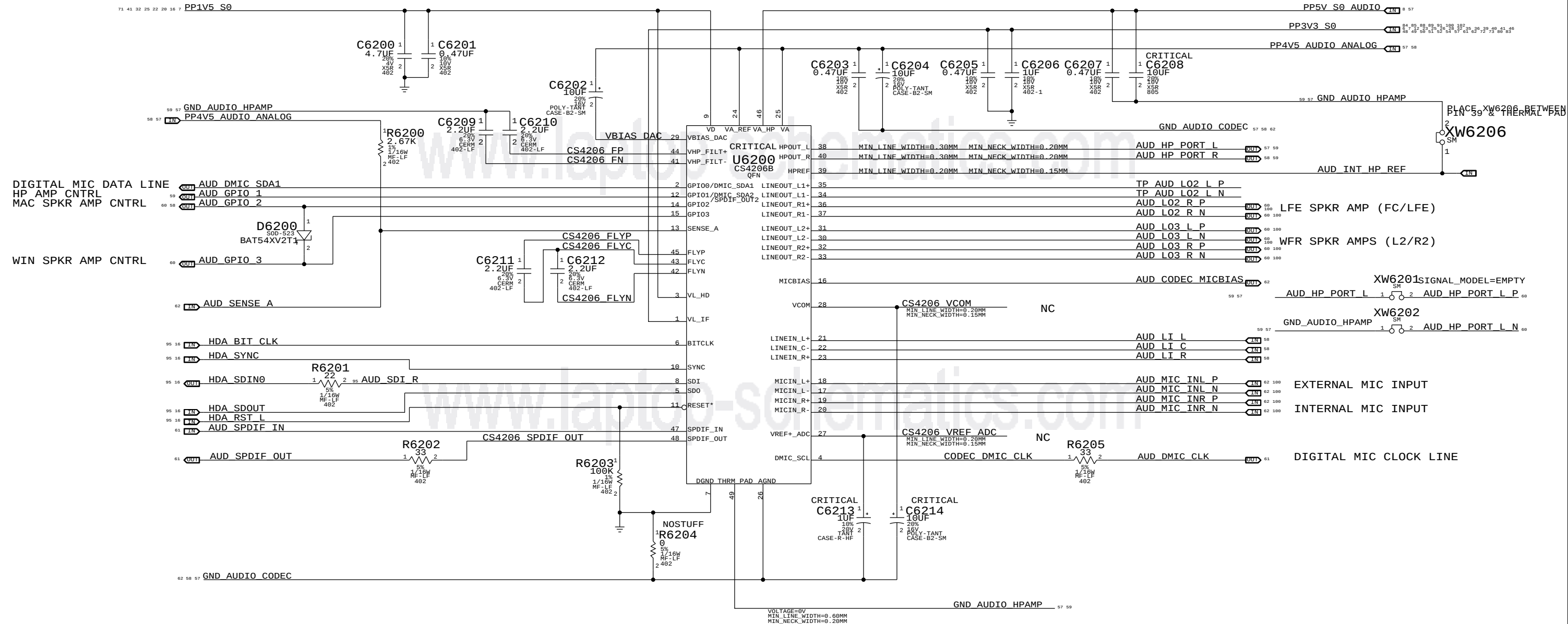
J5815 pin 1 is grounded on keyboard backlight flex

518S0691



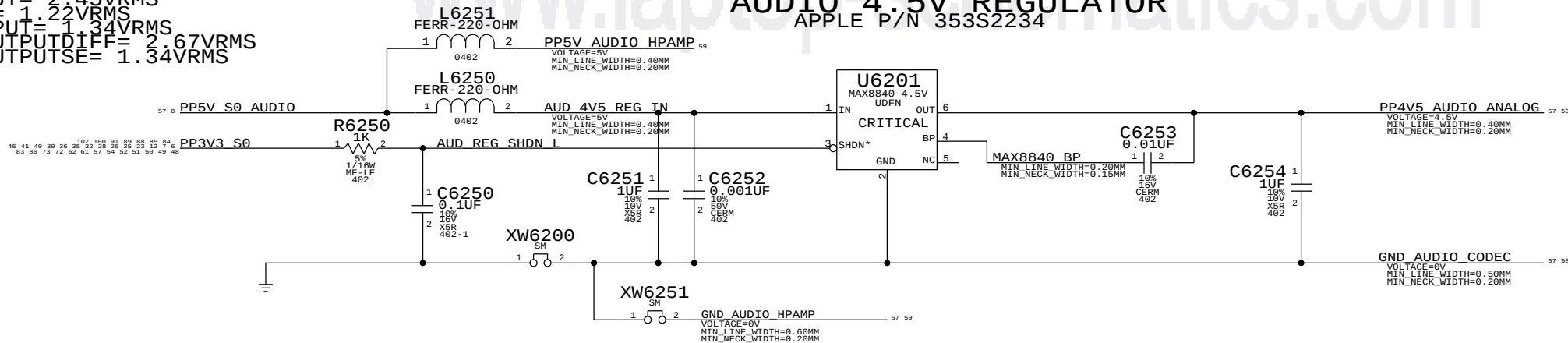


AUDIO CODEC
APPLE P/N 353S3199

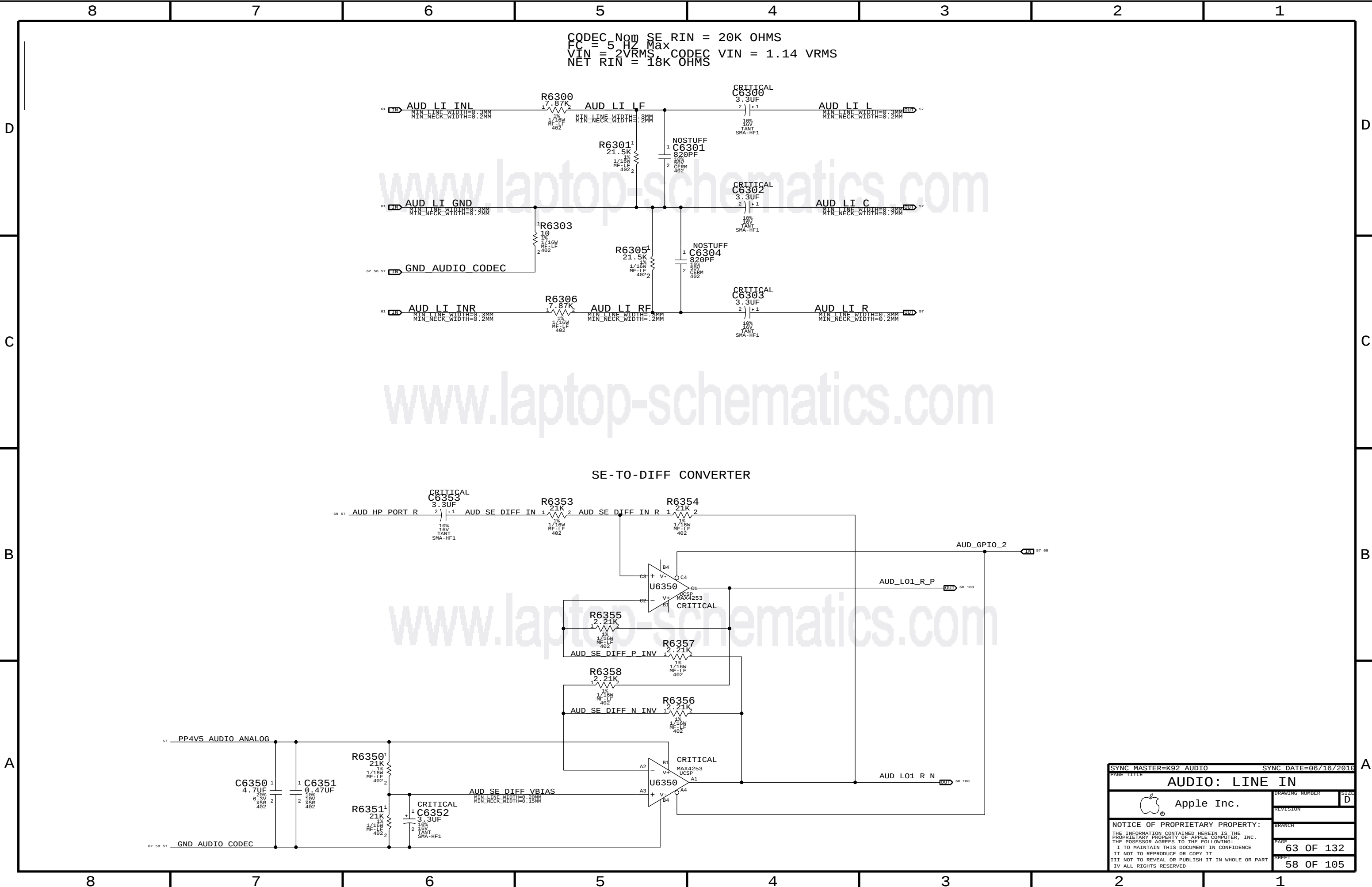


AUDIO 4.5V REGULATOR
APPLE P/N 353S2234

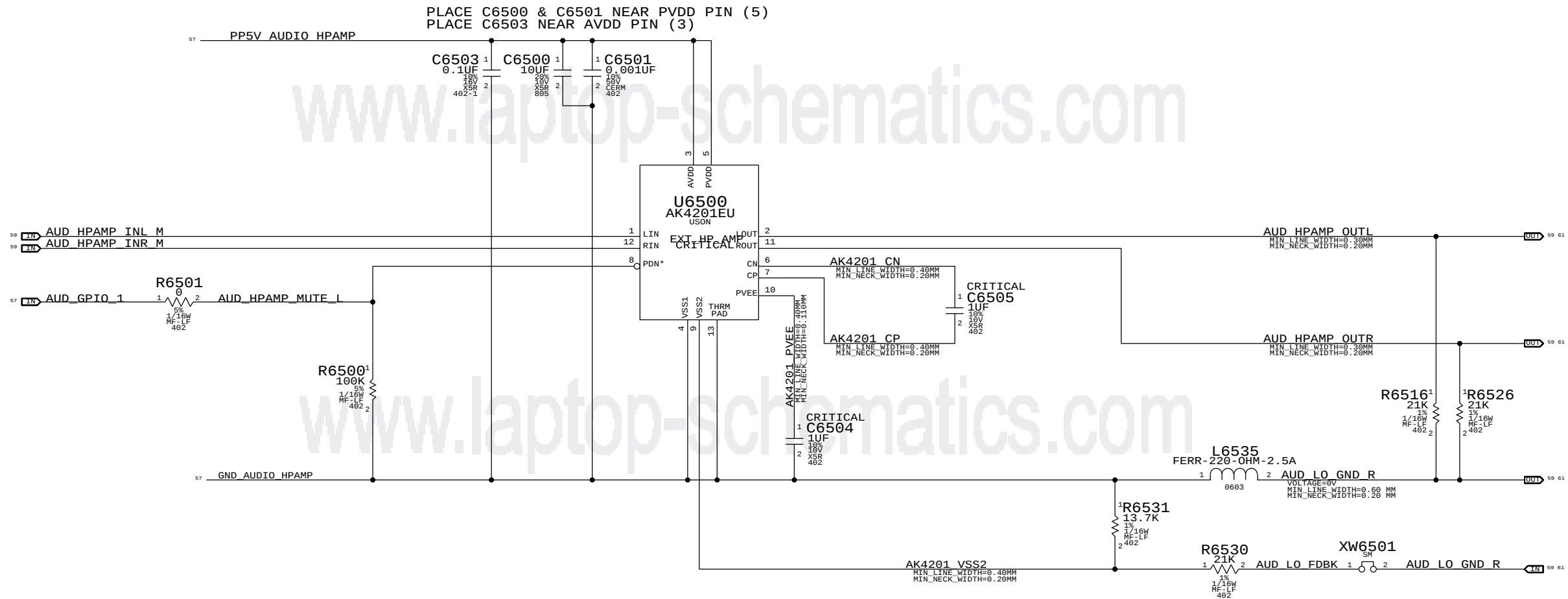
DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

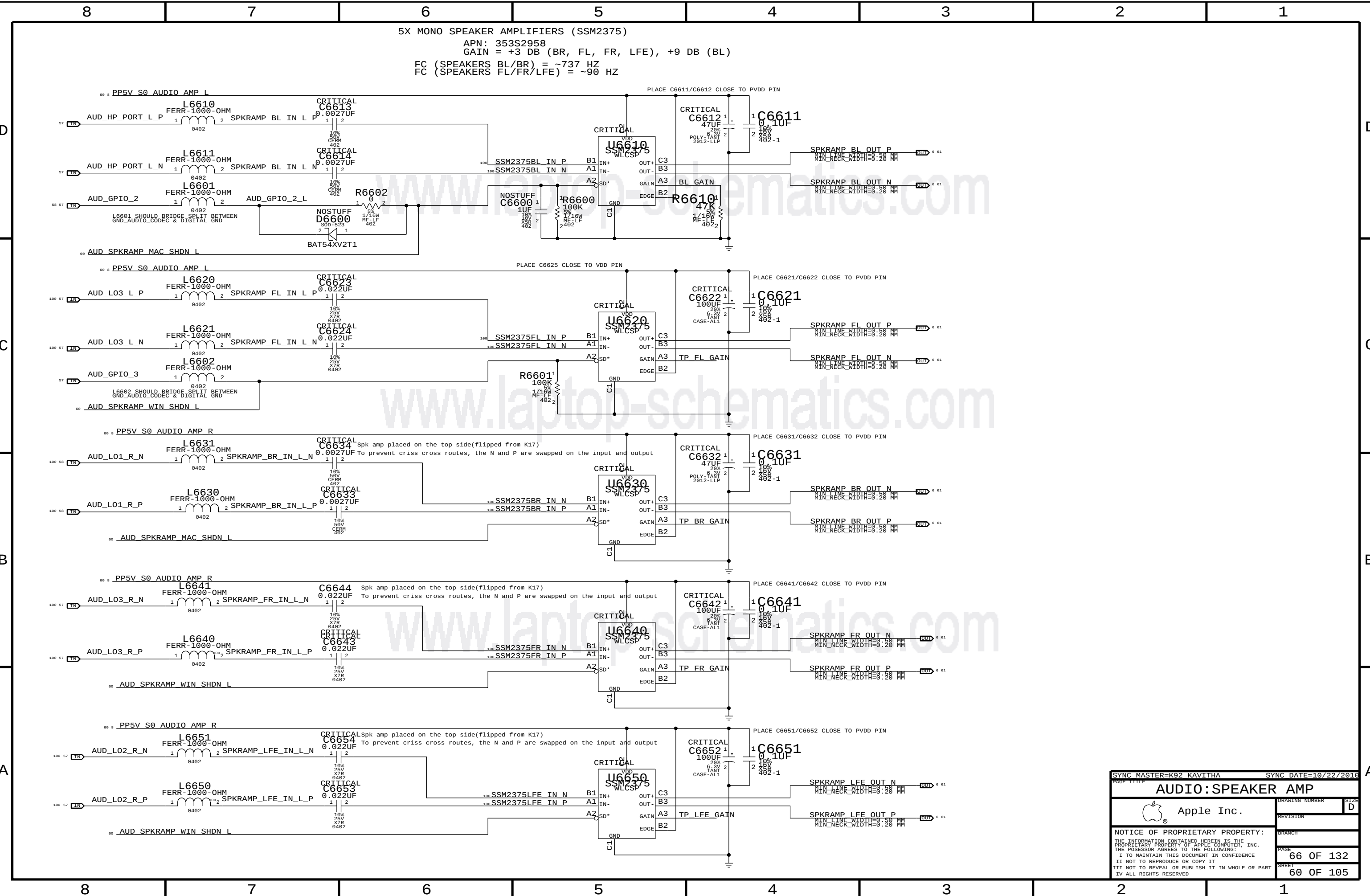


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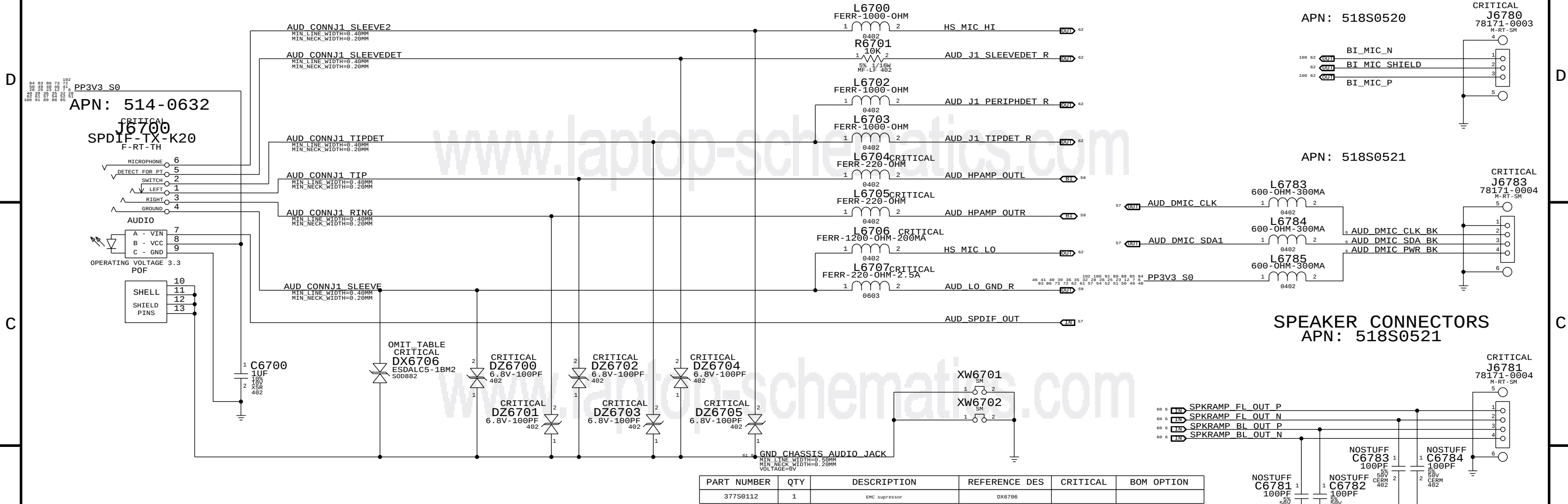
HEADPHONE AMPLIFIER (AK4201)
APN:353S2347
VOLTAGE GAIN:1.53





AUDIO JACK 1 LO/HP JACK, SPDIF TX

MIC CONNECTORS: single anlg mic + 1 dig mic



APN: 518S0520

CRITICAL
J6780
78171-0003
M-RT-SM

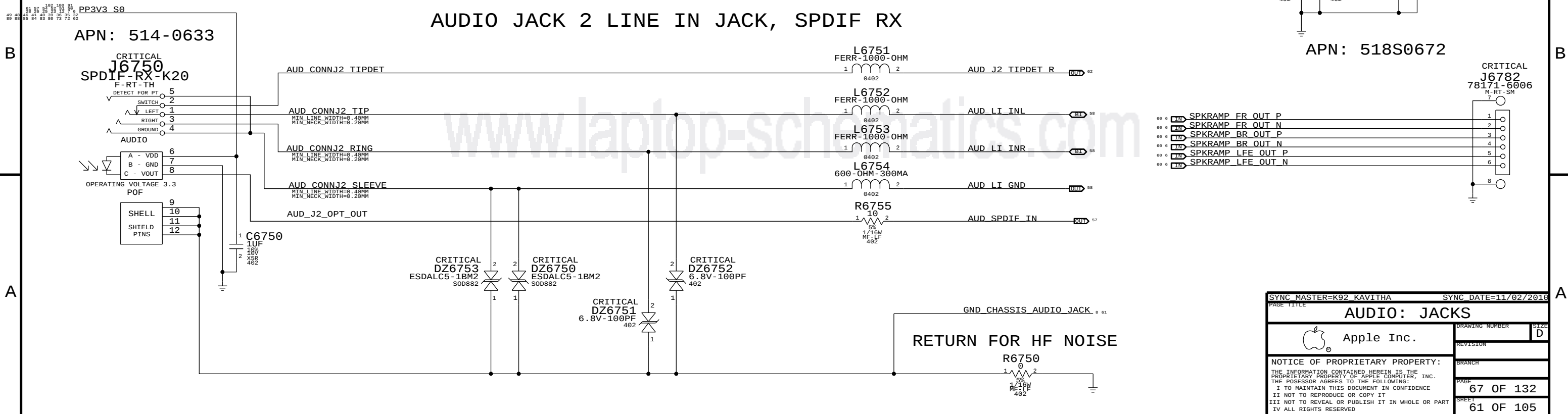
APN: 518S0521

CRITICAL
J6783
78171-0004
M-RT-SM

SPEAKER CONNECTORS
APN: 518S0521

CRITICAL
J6781
78171-0004
M-RT-SM

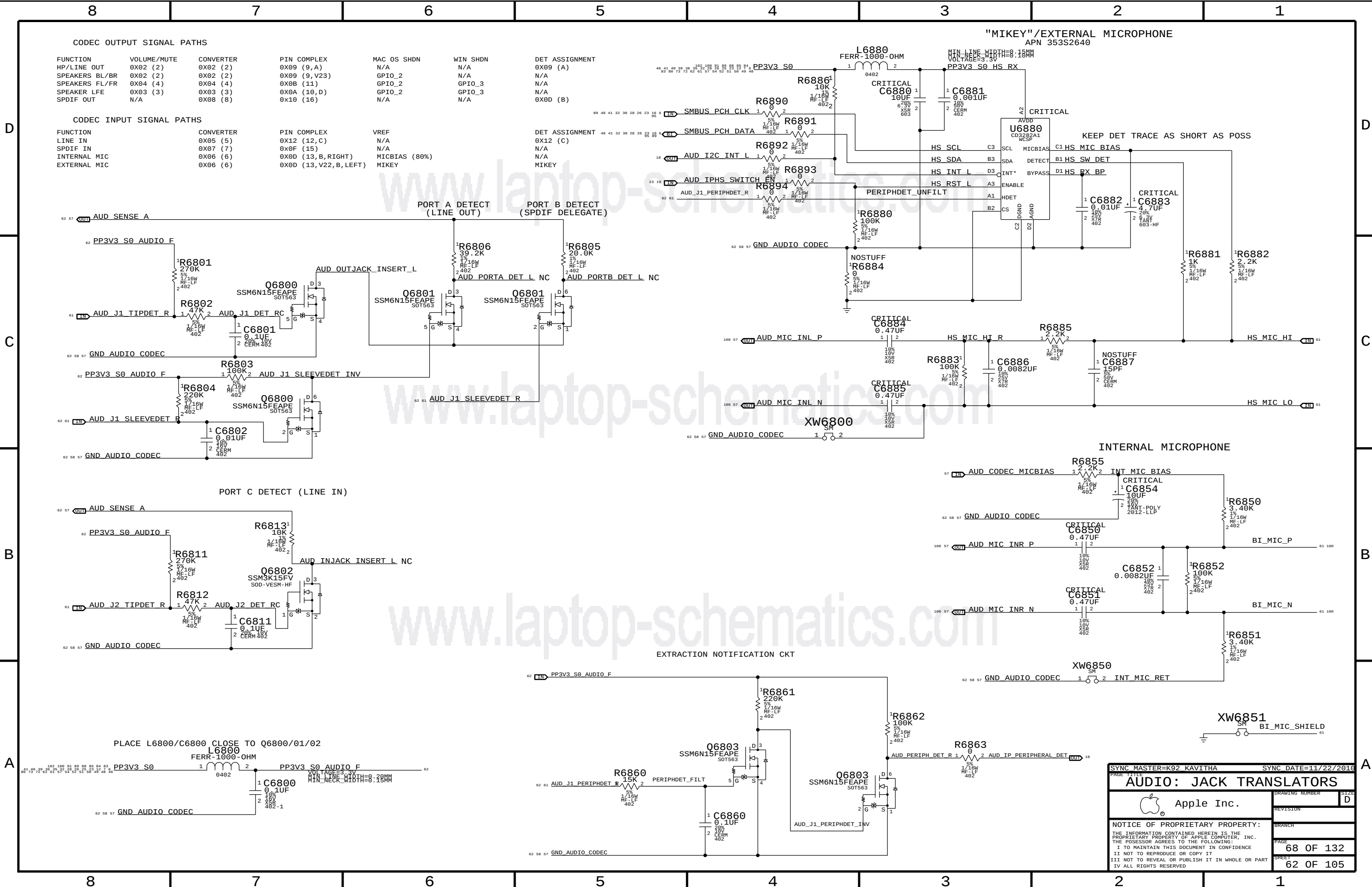
AUDIO JACK 2 LINE IN JACK, SPDIF RX



APN: 518S0672

CRITICAL
J6782
78171-0006
M-RT-SM

SYNC MASTER=K92 KAVITHA		SYNC DATE=11/02/2016	
PAGE TITLE		AUDIO: JACKS	
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CODEC OUTPUT SIGNAL PATHS						
FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC OS SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	N/A	0X09 (A)
SPEAKERS BL/BR	0X02 (2)	0X02 (2)	0X09 (9,V23)	GPIO_2	N/A	N/A
SPEAKERS FL/FR	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_2	GPIO_3	N/A
SPEAKER LFE	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS				
FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X12 (12,C)	N/A	0X12 (C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
INTERNAL MIC	0X06 (6)	0X0D (13,B,RIGHT)	MICBIAS (80%)	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

SYNC MASTER=K92 KAVITHA

SYNC DATE=11/22/2016

AUDIO: JACK TRANSLATORS

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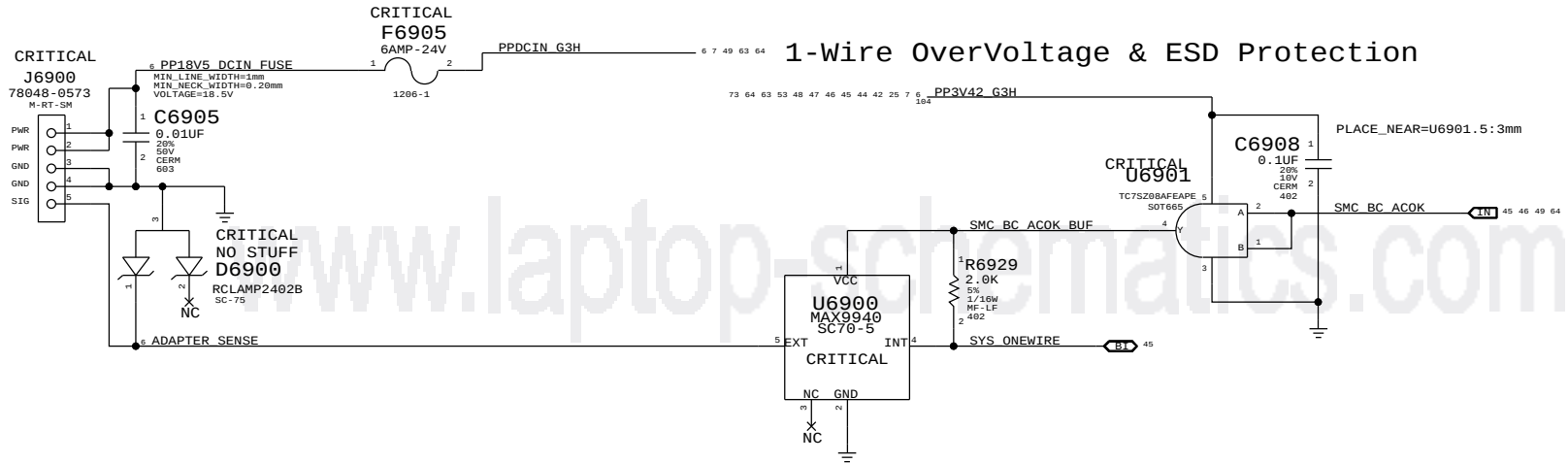
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68 OF 132

REVISION

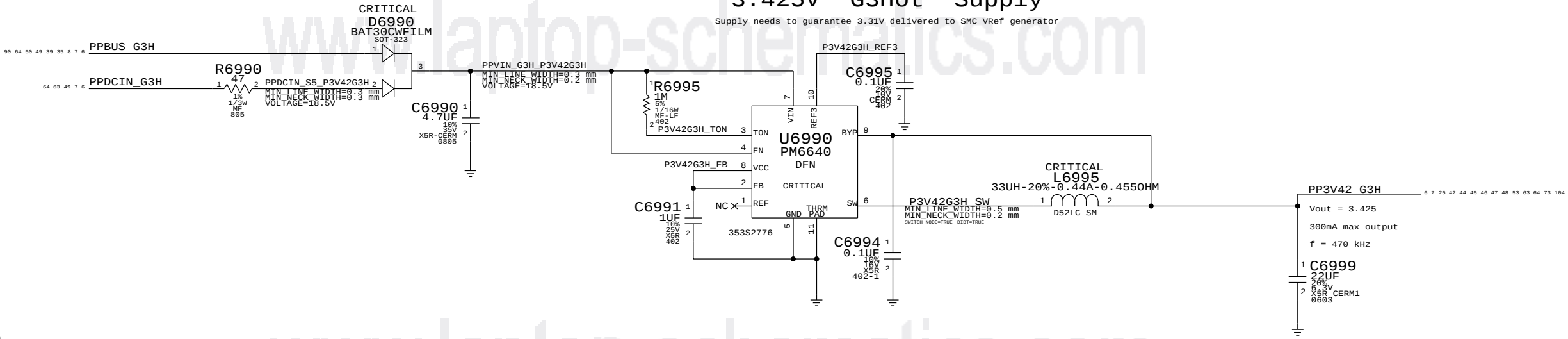
62 OF 105

MagSafe DC Power Jack

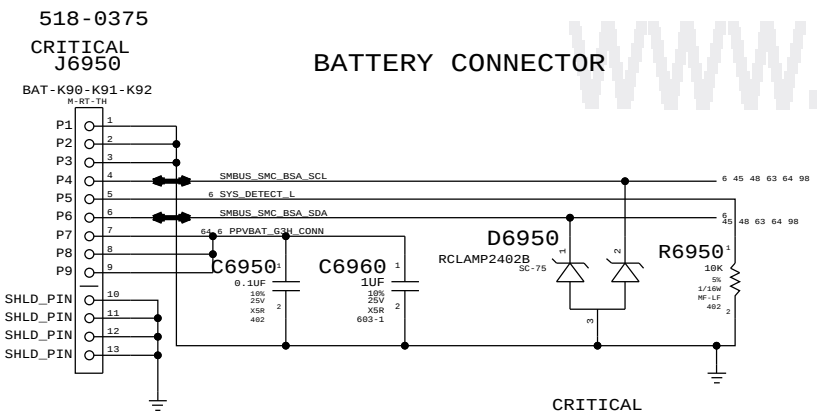


3.425V "G3Hot" Supply

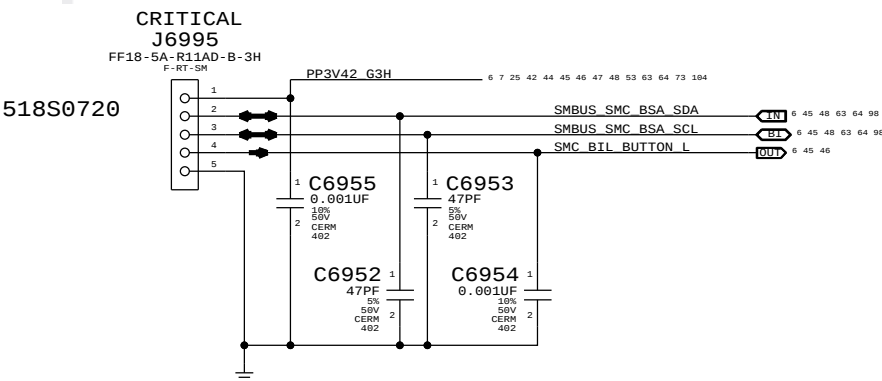
Supply needs to guarantee 3.31V delivered to SMC VRef generator

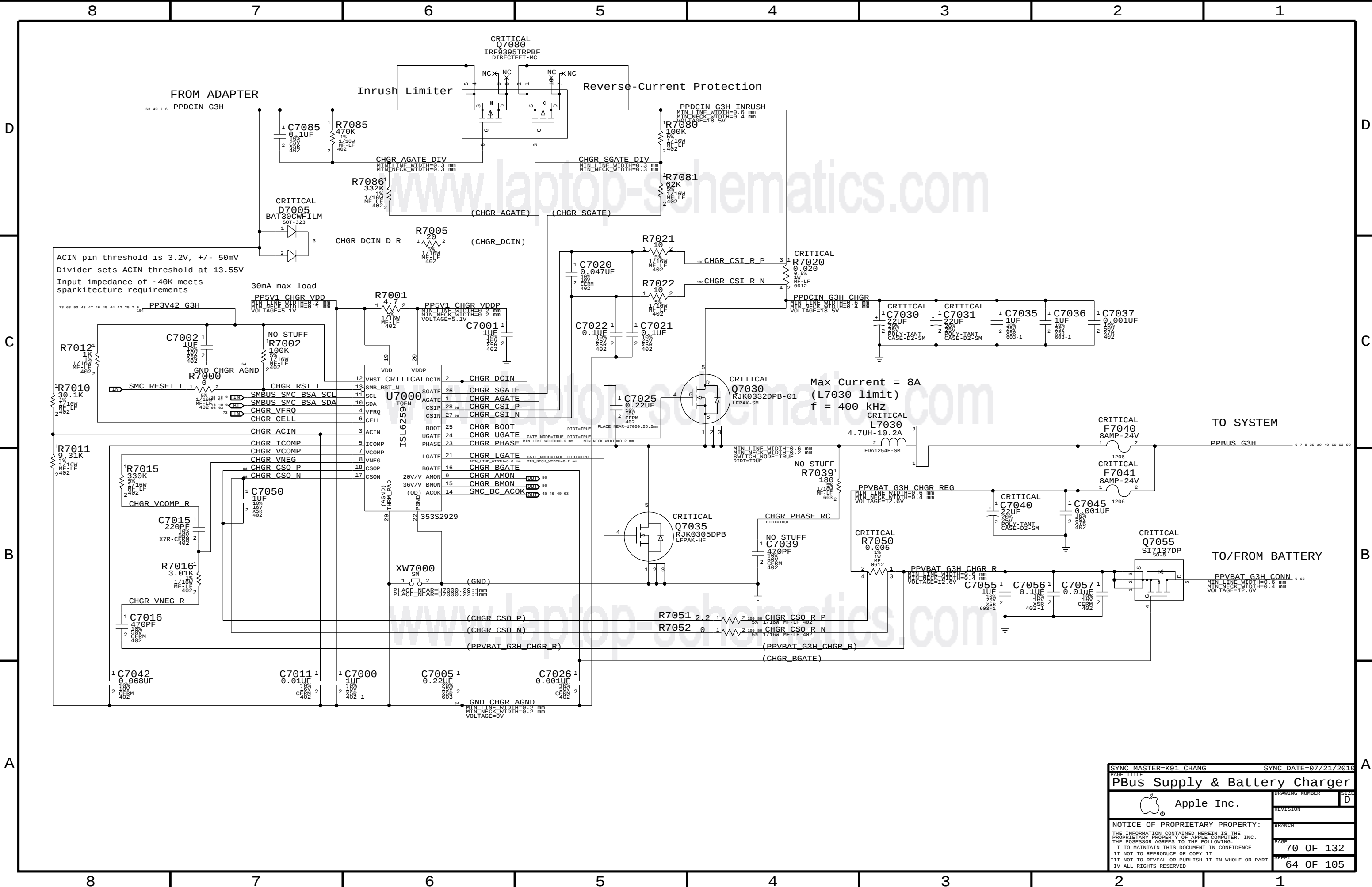


BATTERY CONNECTOR



BIL Connector





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www.laptop-schematics.com

D

D

C

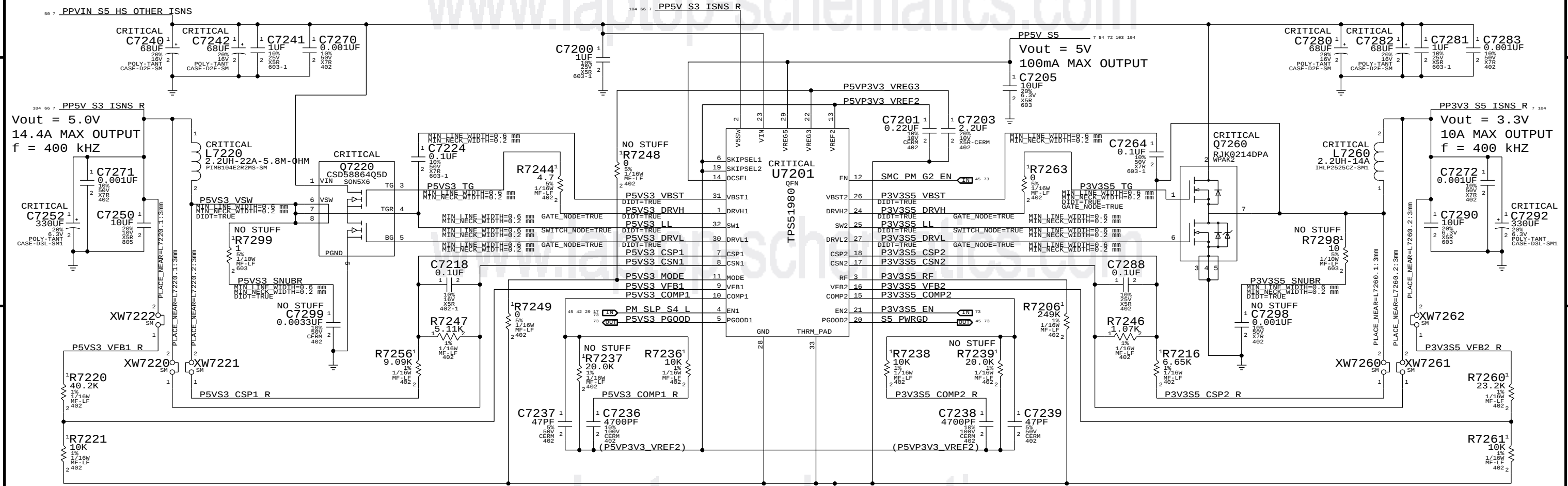
C

B

B

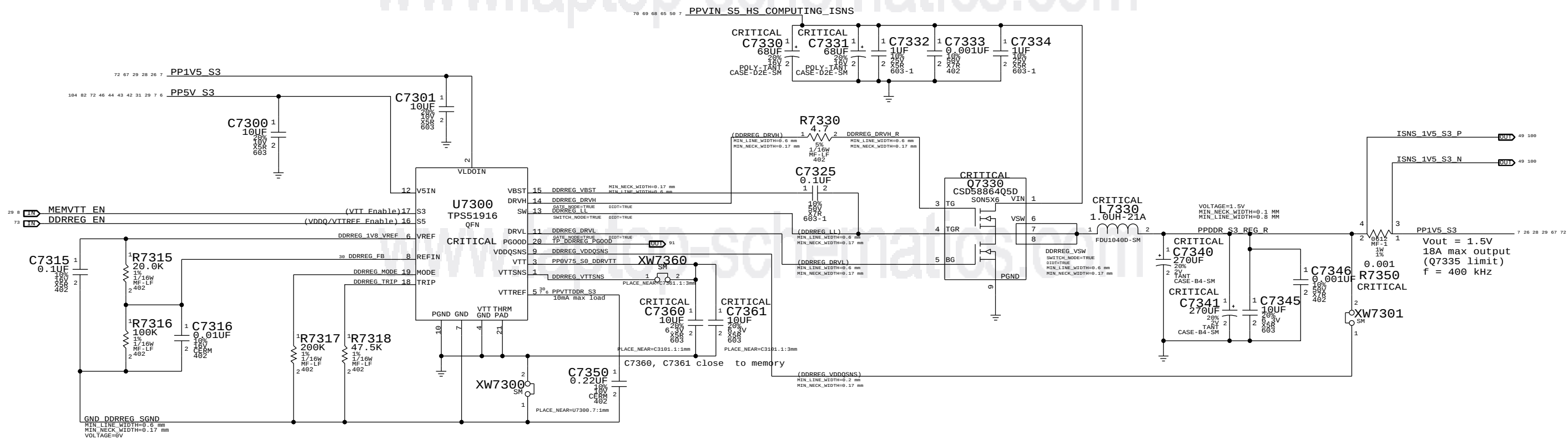
A

A



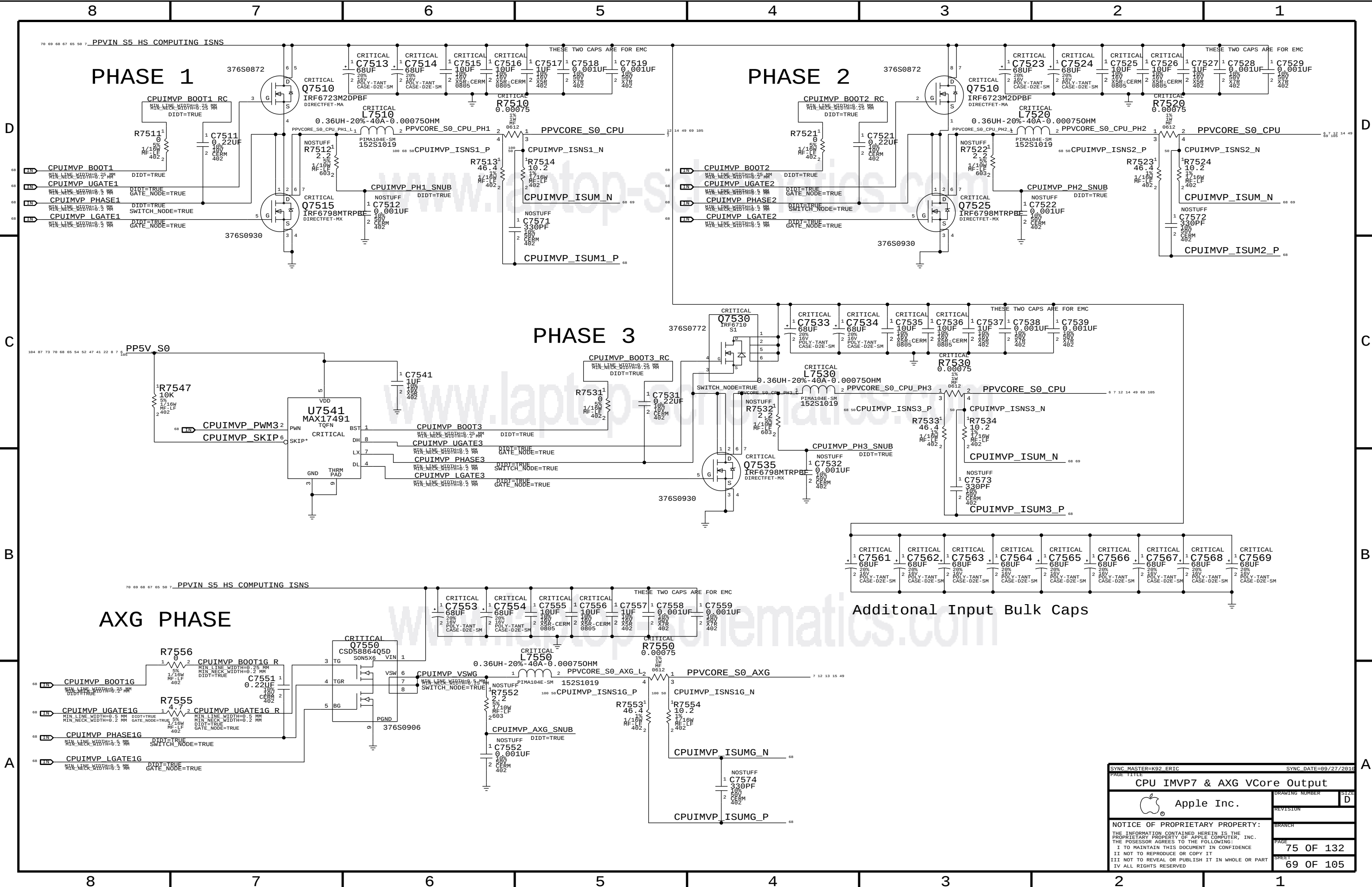
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PAGE TITLE		5V / 3.3V Power Supply	
Apple Inc.		DRAWING NUMBER	SIZE
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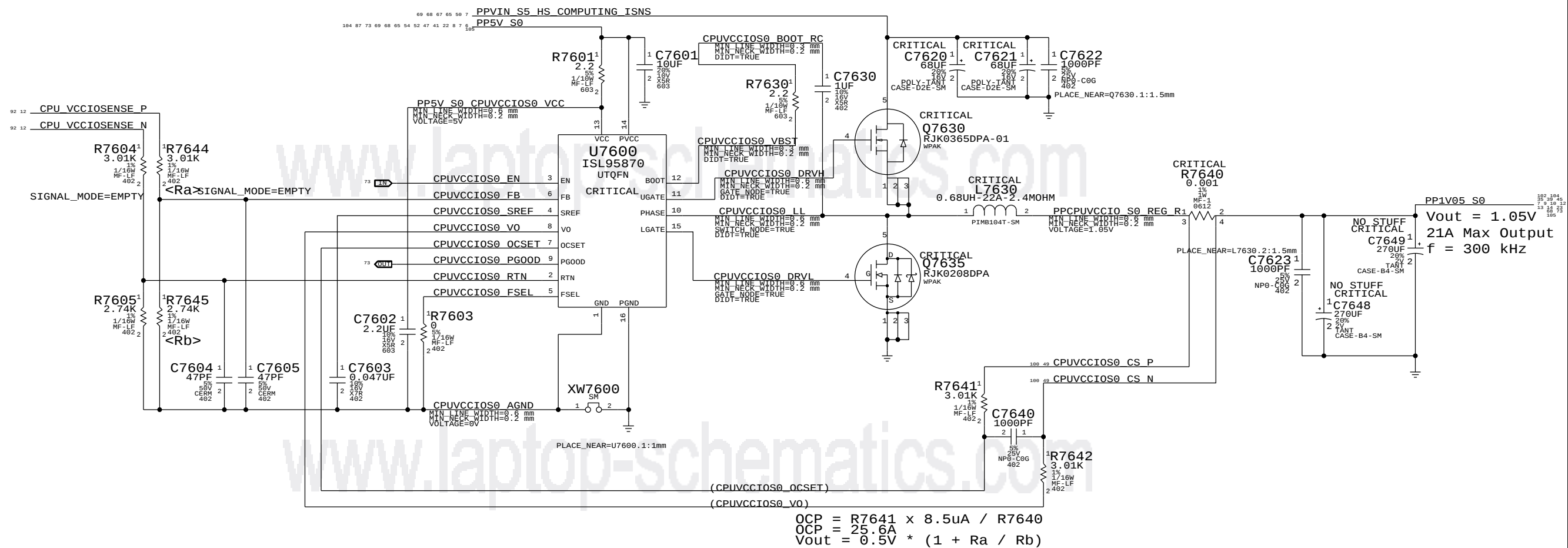
SYNC MASTER=K91 CHANG		SYNC DATE=07/21/2010	
PAGE TITLE		1.5V DDR3 Supply	
Apple Inc.		DRAWING NUMBER	SIZE
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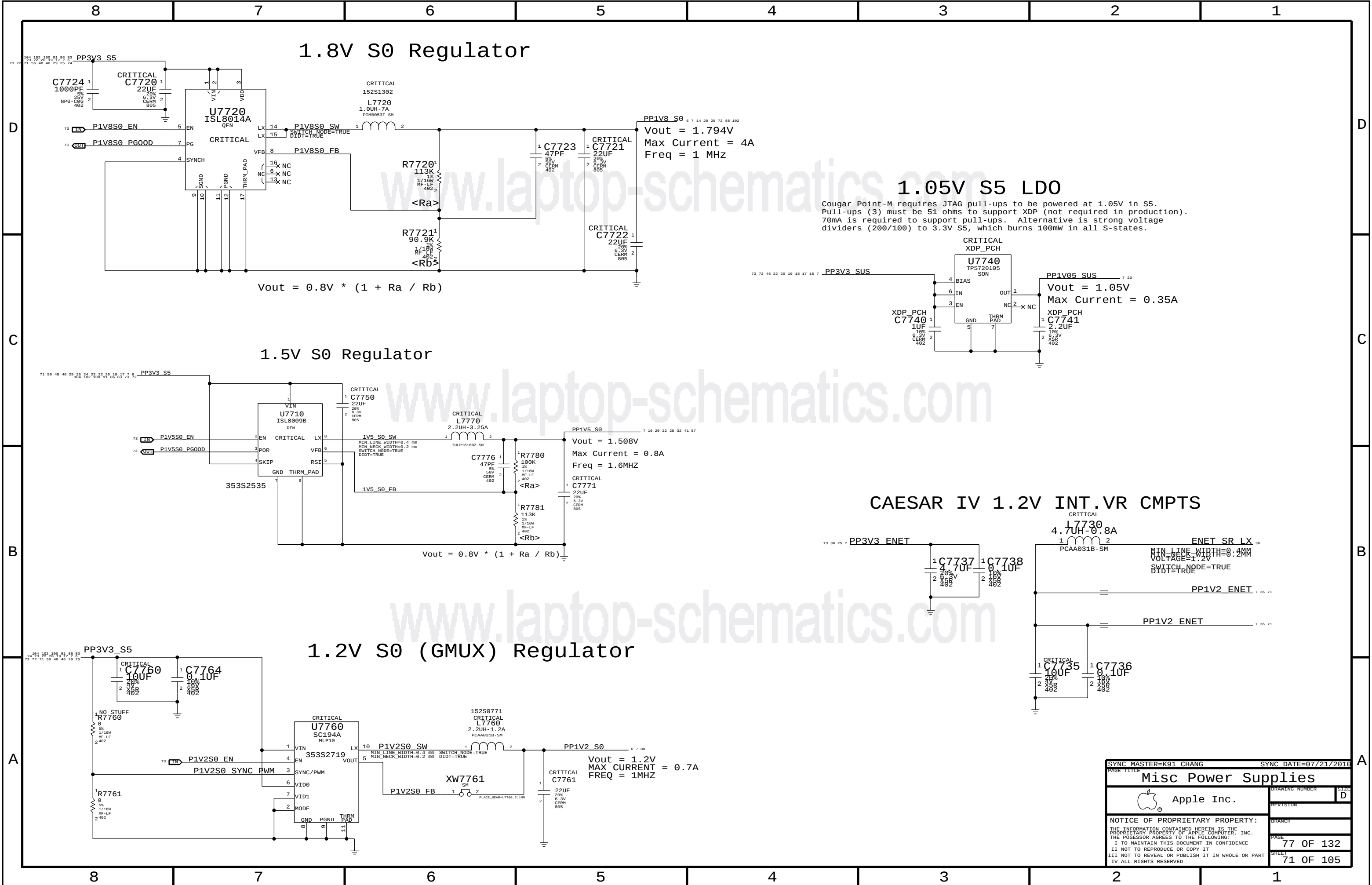
SYNC MASTER=K92 ERIC		SYNC DATE=89/27/2810	
PAGE TITLE		CPU IMVP7 & AXG VCore Output	
Apple Inc.		DRAWING NUMBER	SIZE D
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CPU VCCIO (1.05V S0) Regulator

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SYNC MASTER=K92 ERIC		SYNC DATE=09/23/2010	
PAGE TITLE			
CPU VCCIO (1.05V) Power Supply			
 Apple Inc.		DRAWING NUMBER	SIZE
		REVISION	D
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1.8V S0 Regulator

Vout = 1.794V
Max Current = 4A
Freq = 1 MHz

1.05V S5 LDO

Cougar Point-M requires JTAG pull-ups to be powered at 1.05V in S5. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.

Vout = 1.05V
Max Current = 0.35A

1.5V S0 Regulator

Vout = 1.508V
Max Current = 0.8A
Freq = 1.6MHZ

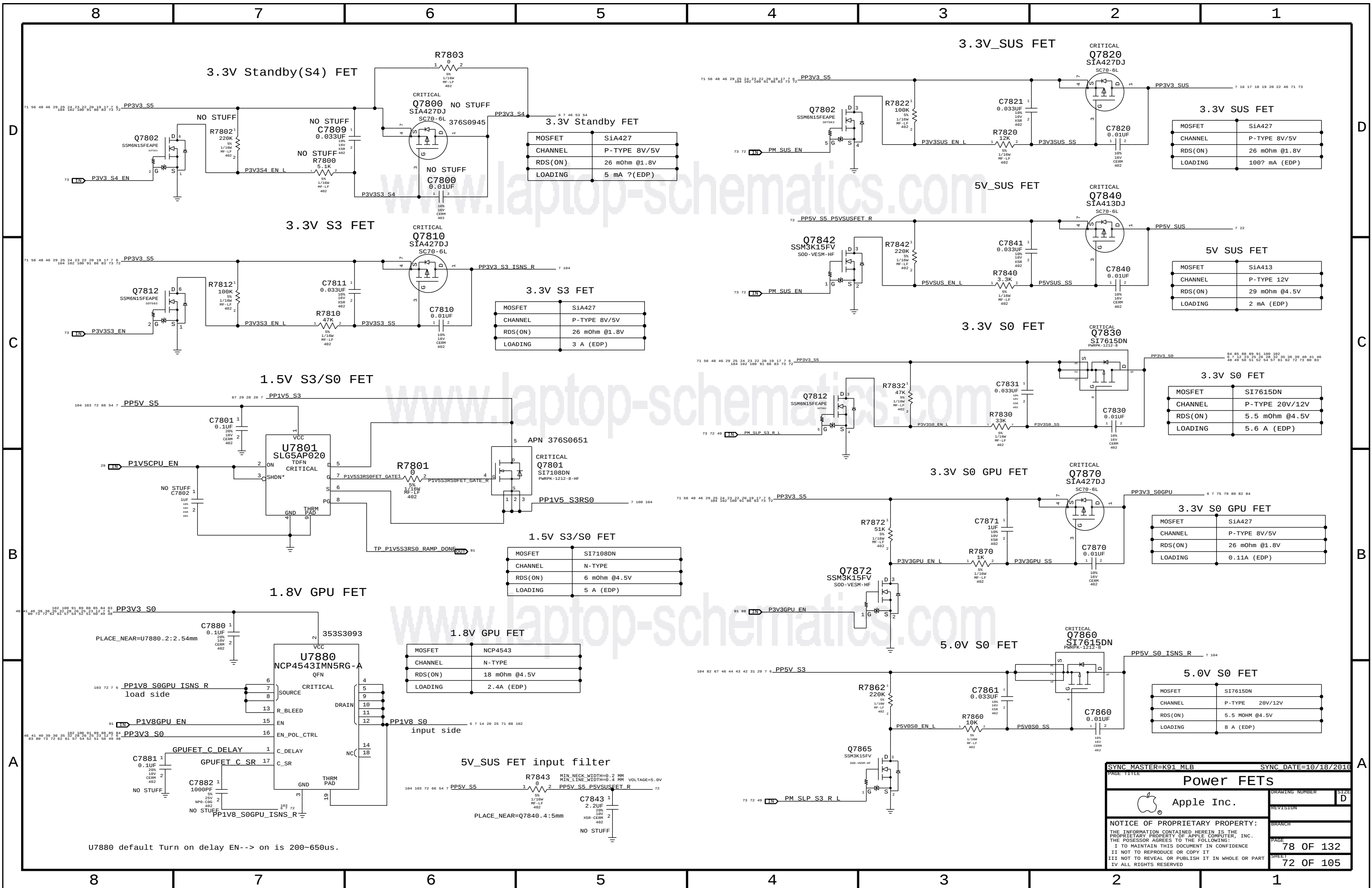
CAESAR IV 1.2V INT.VR CMPTS

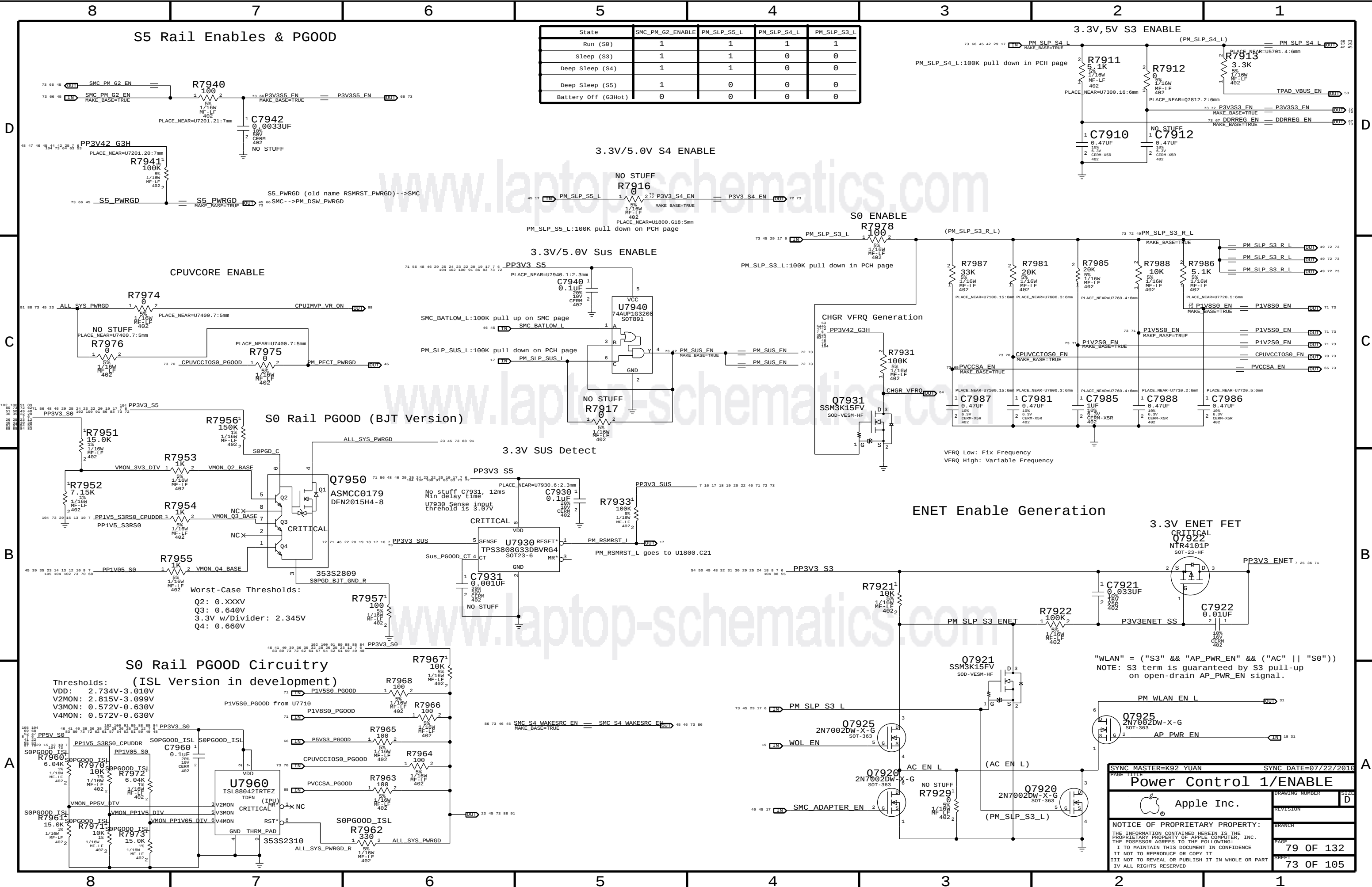
Vout = 1.2V
Max Current = 0.7A
Freq = 1MHz

1.2V S0 (GMUX) Regulator

Vout = 1.2V
MAX CURRENT = 0.7A
FREQ = 1MHZ

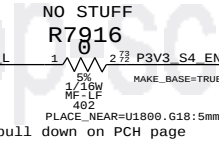
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PAGE TITLE		DRAWING NUMBER	
Misc Power Supplies		SIZE	
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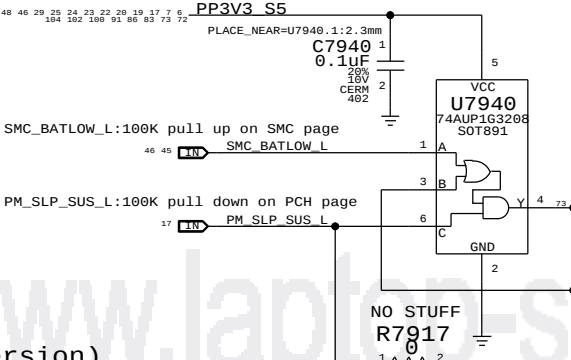


State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	0	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

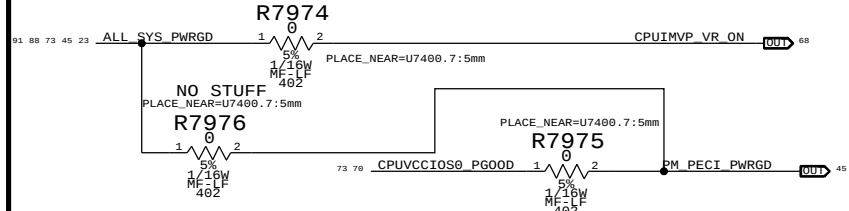
3.3V/5.0V S4 ENABLE



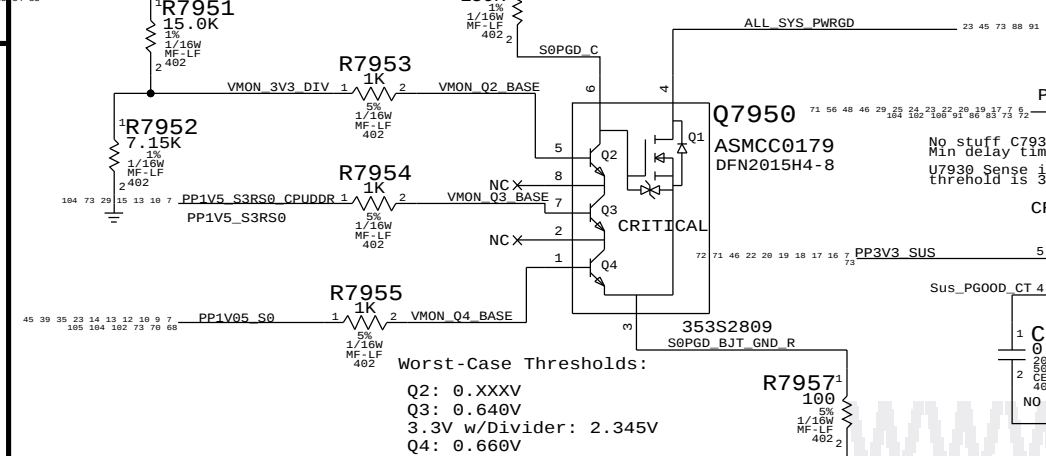
3.3V/5.0V Sus ENABLE



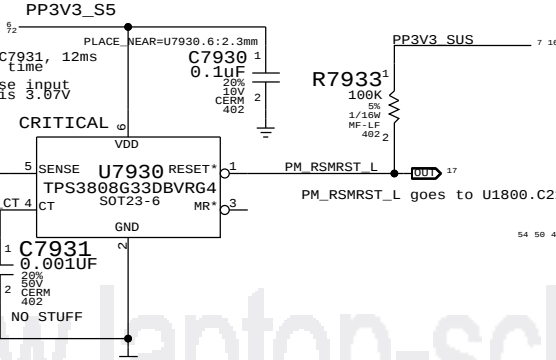
CPUVCORE ENABLE



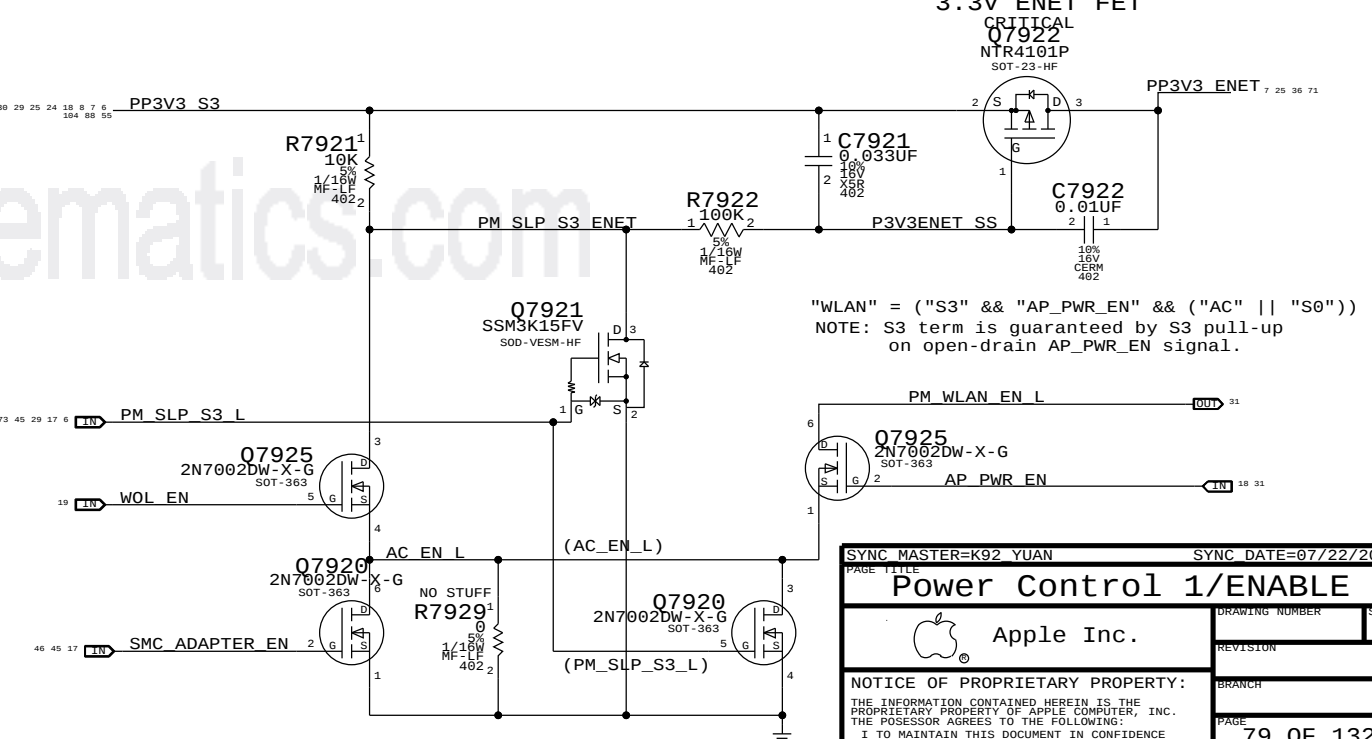
S0 Rail PG00D (BJT Version)



3.3V SUS Detect

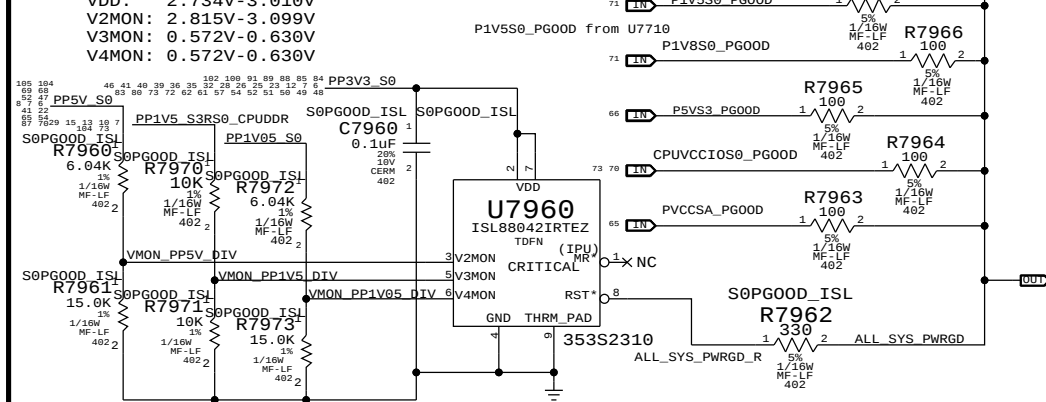


ENET Enable Generation



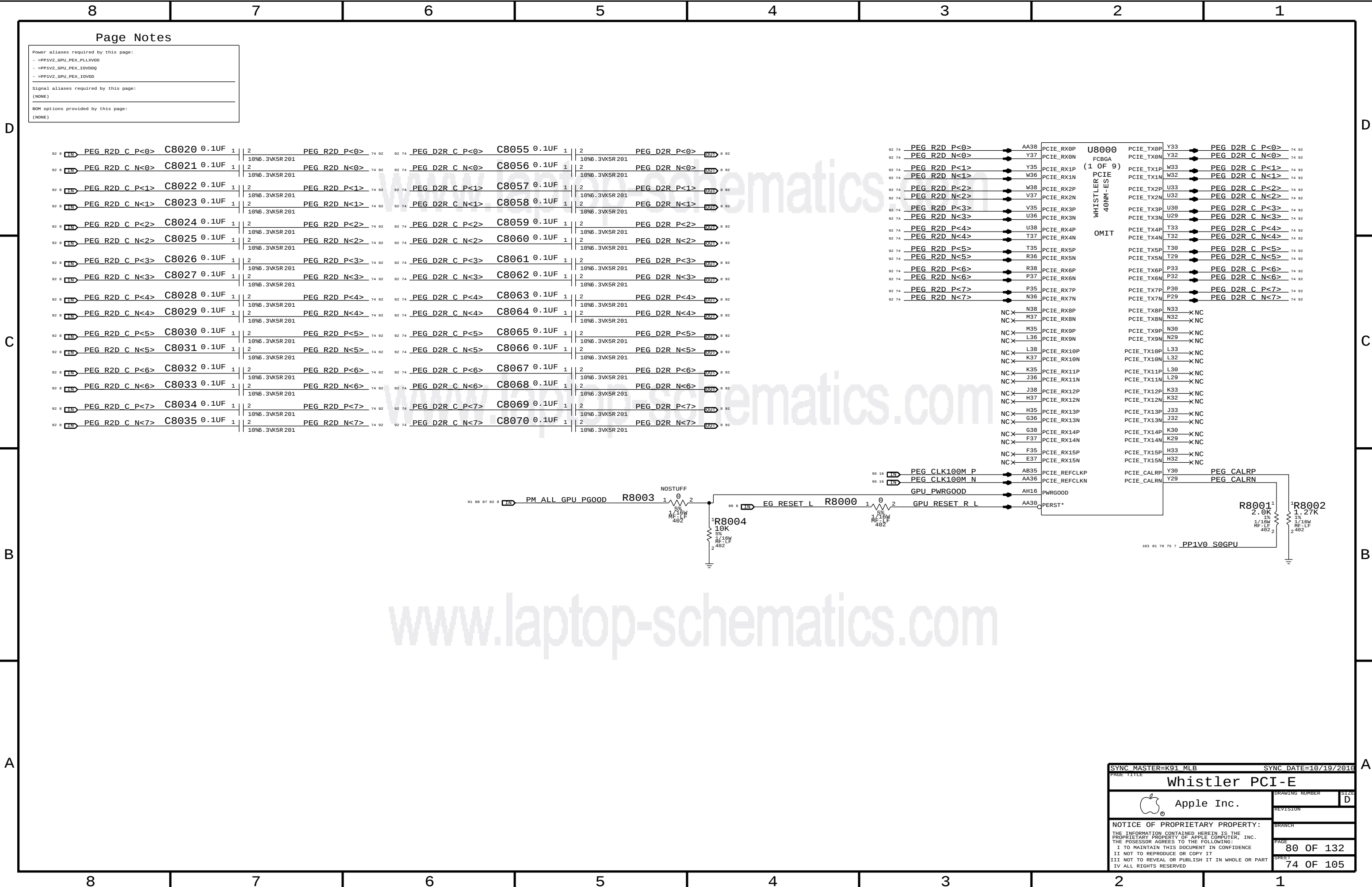
S0 Rail PG00D Circuitry

(ISL Version in development)



"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

SYNC MASTER=K92 YUAN		SYNC DATE=07/22/2016	
Power Control 1/ENABLE		DRAWING NUMBER	
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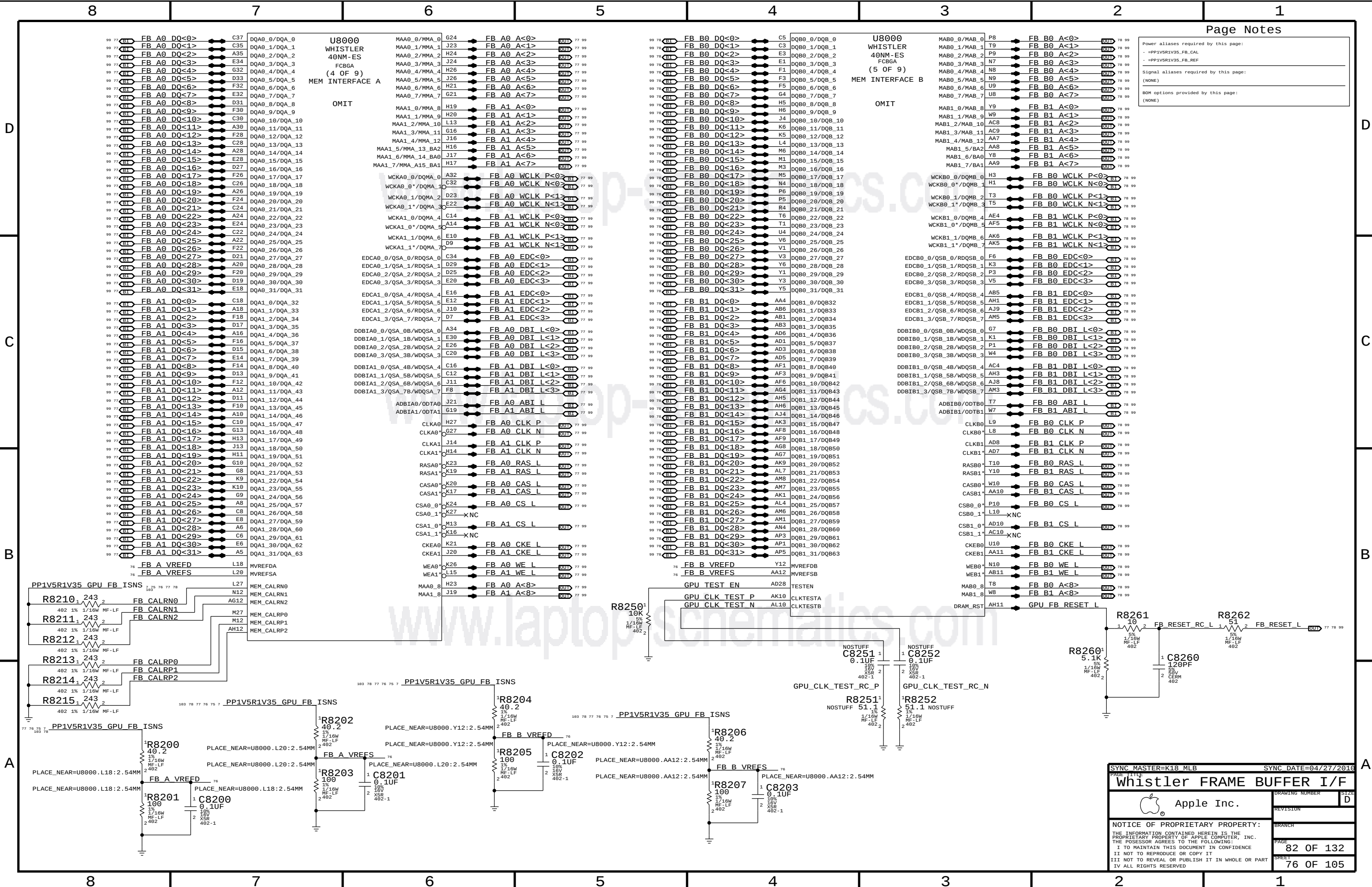
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)



Page Notes	
Power aliases required by this page:	
- #PP1V5R1V35_FB_CAL	
- #PP1V5R1V35_FB_REF	
Signal aliases required by this page:	
(NONE)	
BOM options provided by this page:	
(NONE)	

SYNC MASTER=K18 MLB

SYNC DATE=04/27/2016

Whistler FRAME BUFFER I/F

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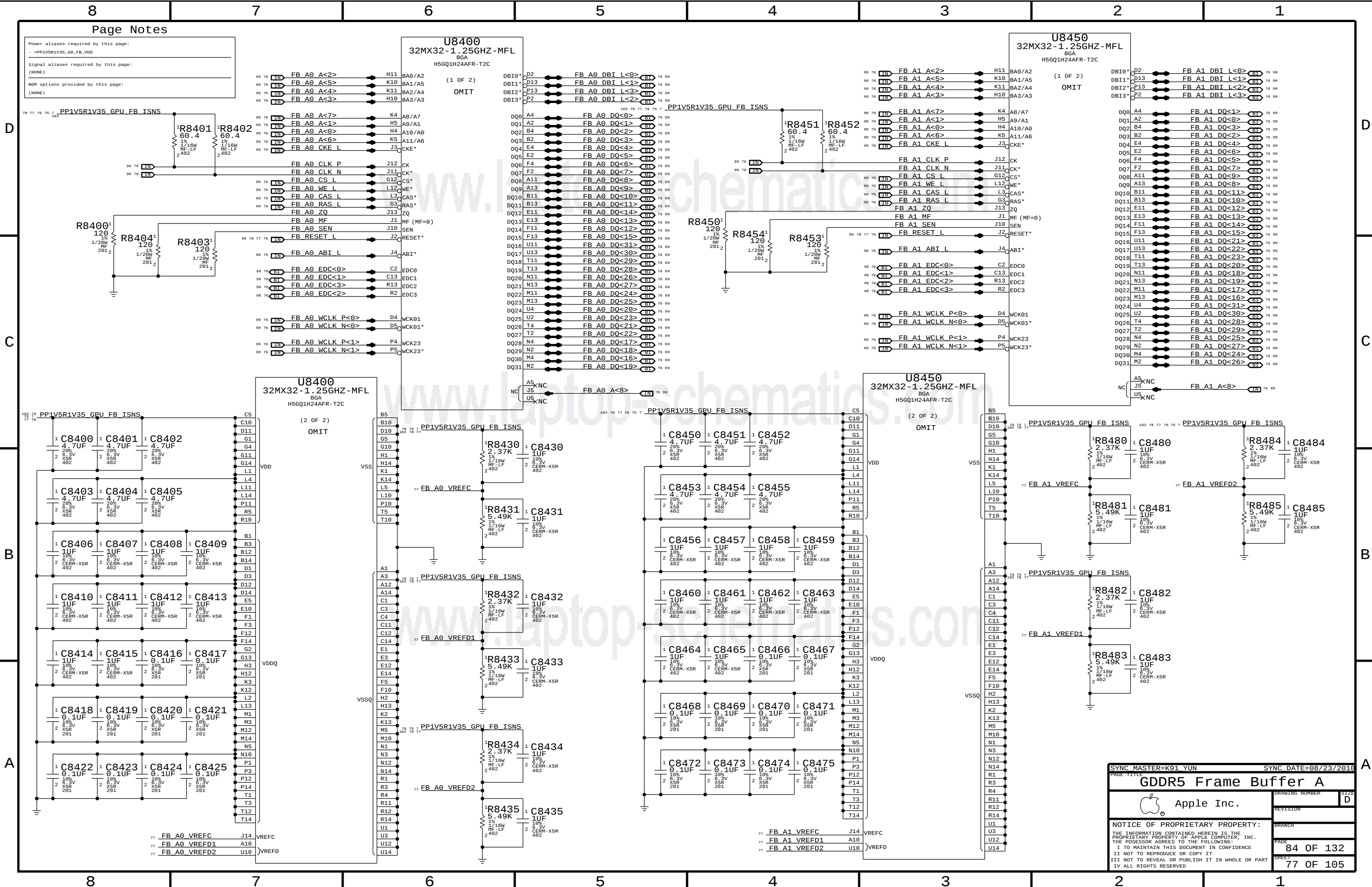
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Power aliases required by this page:
- PP1V5R1V35_GPU_FB_ISNS

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

U8400		32MX32-1.25GHZ-MFL		BGA		H5GQ1H24AFR-T2C	
(1 OF 2)		OMIT					
DBI0*	D2	FB A0 DBI L<0>	B1	76	99		
DBI1*	D13	FB A0 DBI L<1>	B1	76	99		
DBI2*	P13	FB A0 DBI L<3>	B1	76	99		
DBI3*	P2	FB A0 DBI L<2>	B1	76	99		
DQ0	A4	FB A0 DQ<0>	B1	76	99		
DQ1	A2	FB A0 DQ<1>	B1	76	99		
DQ2	B4	FB A0 DQ<2>	B1	76	99		
DQ3	B2	FB A0 DQ<3>	B1	76	99		
DQ4	E4	FB A0 DQ<4>	B1	76	99		
DQ5	E2	FB A0 DQ<5>	B1	76	99		
DQ6	F4	FB A0 DQ<6>	B1	76	99		
DQ7	F2	FB A0 DQ<7>	B1	76	99		
DQ8	A11	FB A0 DQ<8>	B1	76	99		
DQ9	A13	FB A0 DQ<9>	B1	76	99		
DQ10	B11	FB A0 DQ<10>	B1	76	99		
DQ11	B13	FB A0 DQ<11>	B1	76	99		
DQ12	E11	FB A0 DQ<12>	B1	76	99		
DQ13	E13	FB A0 DQ<13>	B1	76	99		
DQ14	F11	FB A0 DQ<14>	B1	76	99		
DQ15	F13	FB A0 DQ<15>	B1	76	99		
DQ16	U11	FB A0 DQ<16>	B1	76	99		
DQ17	U13	FB A0 DQ<17>	B1	76	99		
DQ18	T11	FB A0 DQ<18>	B1	76	99		
DQ19	T13	FB A0 DQ<19>	B1	76	99		
DQ20	N11	FB A0 DQ<20>	B1	76	99		
DQ21	N13	FB A0 DQ<21>	B1	76	99		
DQ22	M11	FB A0 DQ<22>	B1	76	99		
DQ23	M13	FB A0 DQ<23>	B1	76	99		
DQ24	U4	FB A0 DQ<24>	B1	76	99		
DQ25	U2	FB A0 DQ<25>	B1	76	99		
DQ26	T4	FB A0 DQ<26>	B1	76	99		
DQ27	T2	FB A0 DQ<27>	B1	76	99		
DQ28	N4	FB A0 DQ<28>	B1	76	99		
DQ29	N2	FB A0 DQ<29>	B1	76	99		
DQ30	M4	FB A0 DQ<30>	B1	76	99		
DQ31	M2	FB A0 DQ<31>	B1	76	99		

U8450		32MX32-1.25GHZ-MFL		BGA		H5GQ1H24AFR-T2C	
(2 OF 2)		OMIT					

SYNC MASTER=K91 YUN

SYNC DATE=08/23/2016

GDDR5 Frame Buffer A

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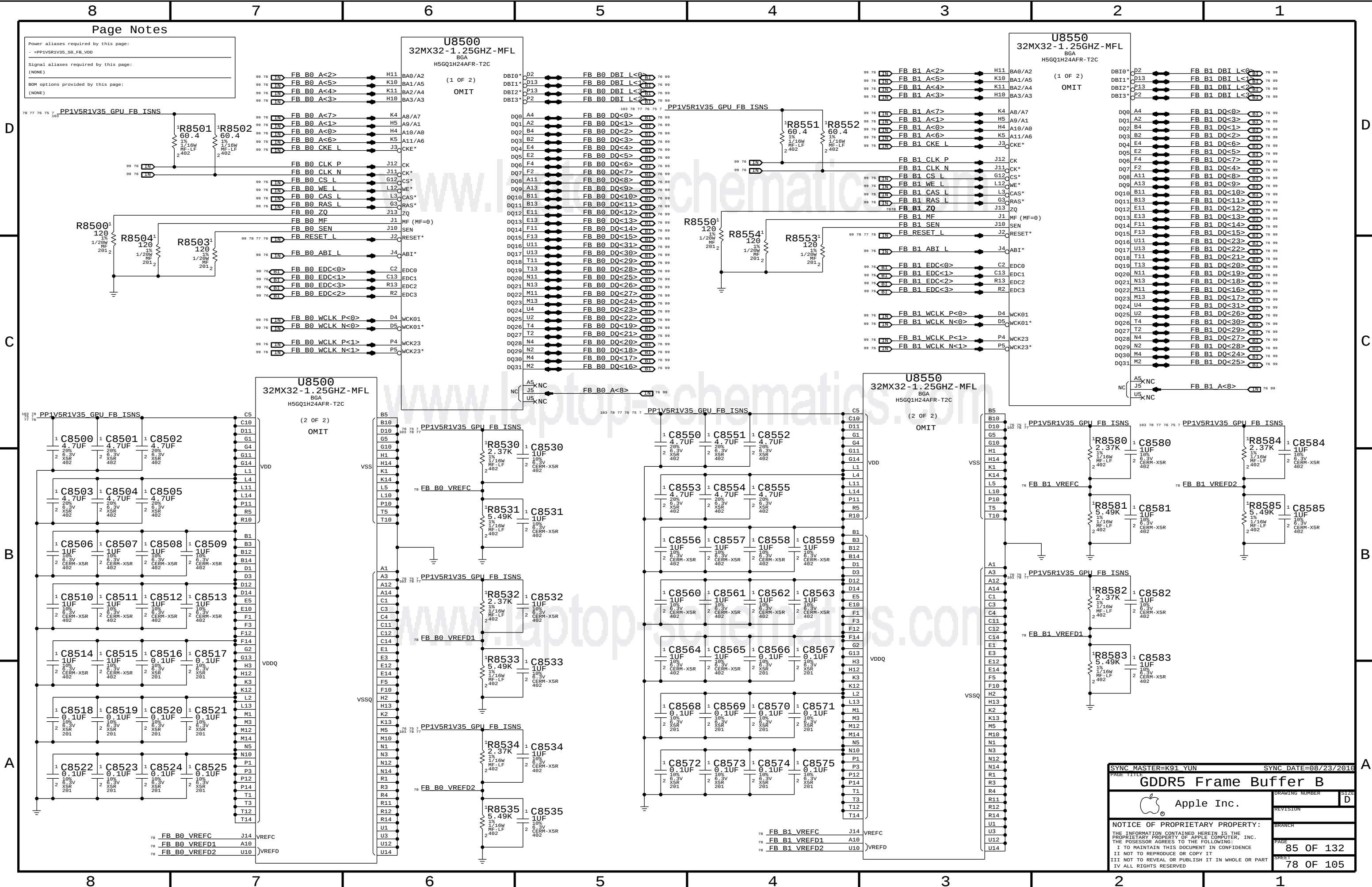
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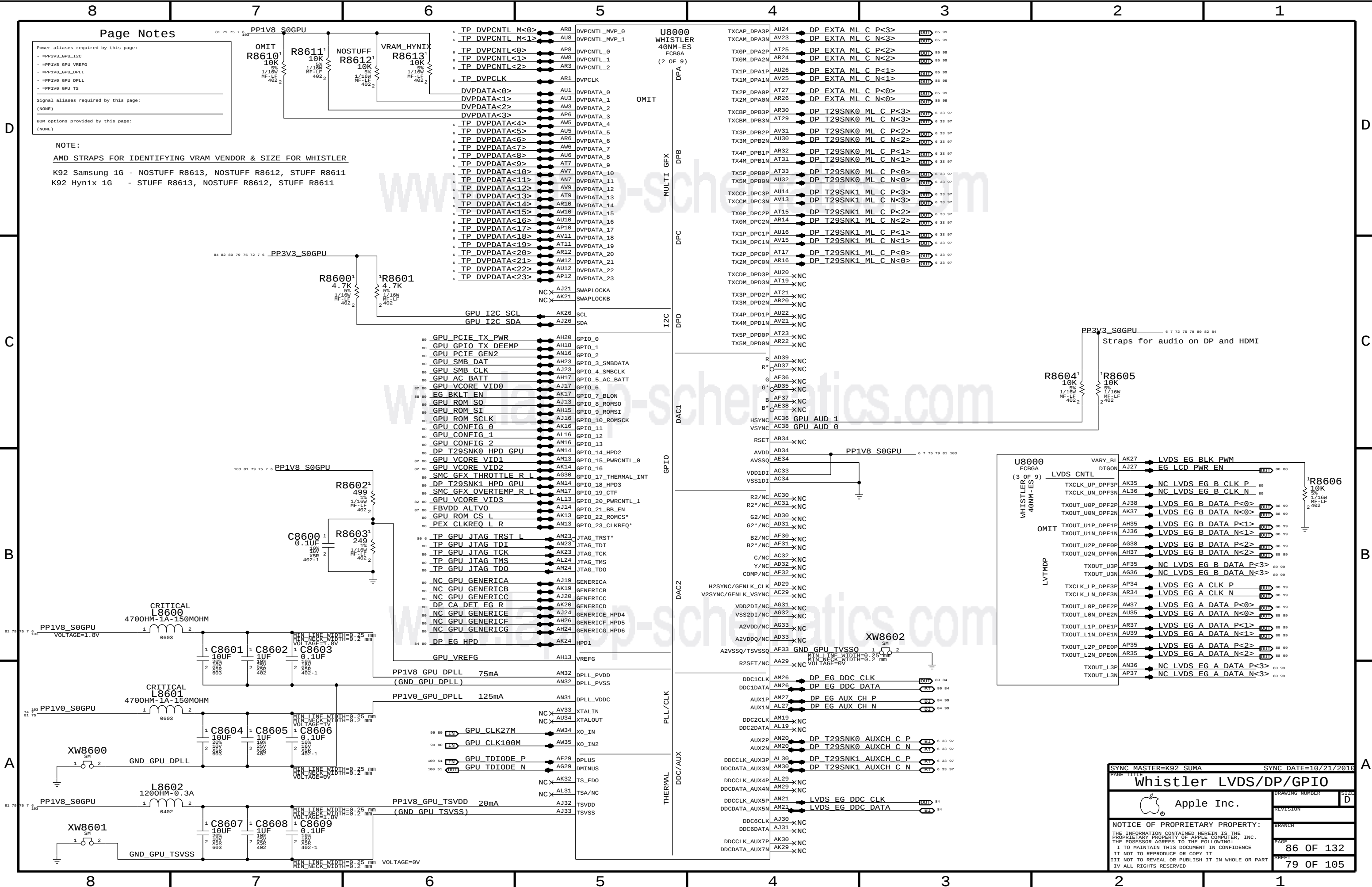
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BOM options provided by this page:
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32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT

U8500
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
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PAGE TITLE			
GDDR5 Frame Buffer B			
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Page Notes

Power aliases required by this page:

- =PP3V3_GPU_I2C
- =PP1V8_GPU_VREFG
- =PP1V8_GPU_DPLL
- =PP1V0_GPU_DPLL
- =PP1V0_GPU_TS

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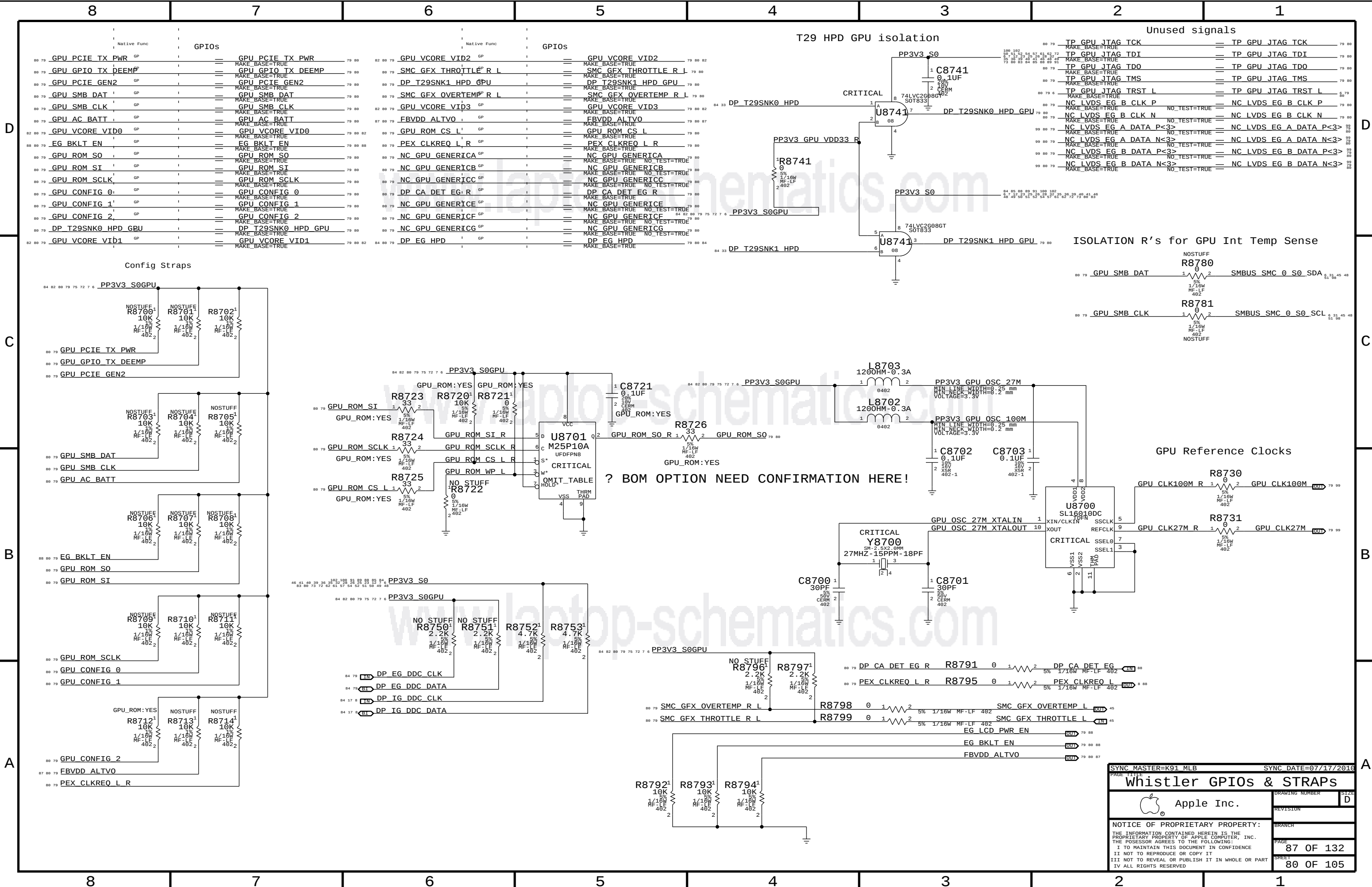
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NOTE:

AMD STRAPS FOR IDENTIFYING VRAM VENDOR & SIZE FOR WHISTLER

K92 Samsung 1G - NOSTUFF R8613, NOSTUFF R8612, STUFF R8611

K92 Hynix 1G - STUFF R8613, NOSTUFF R8612, STUFF R8611



Power aliases required by this page:

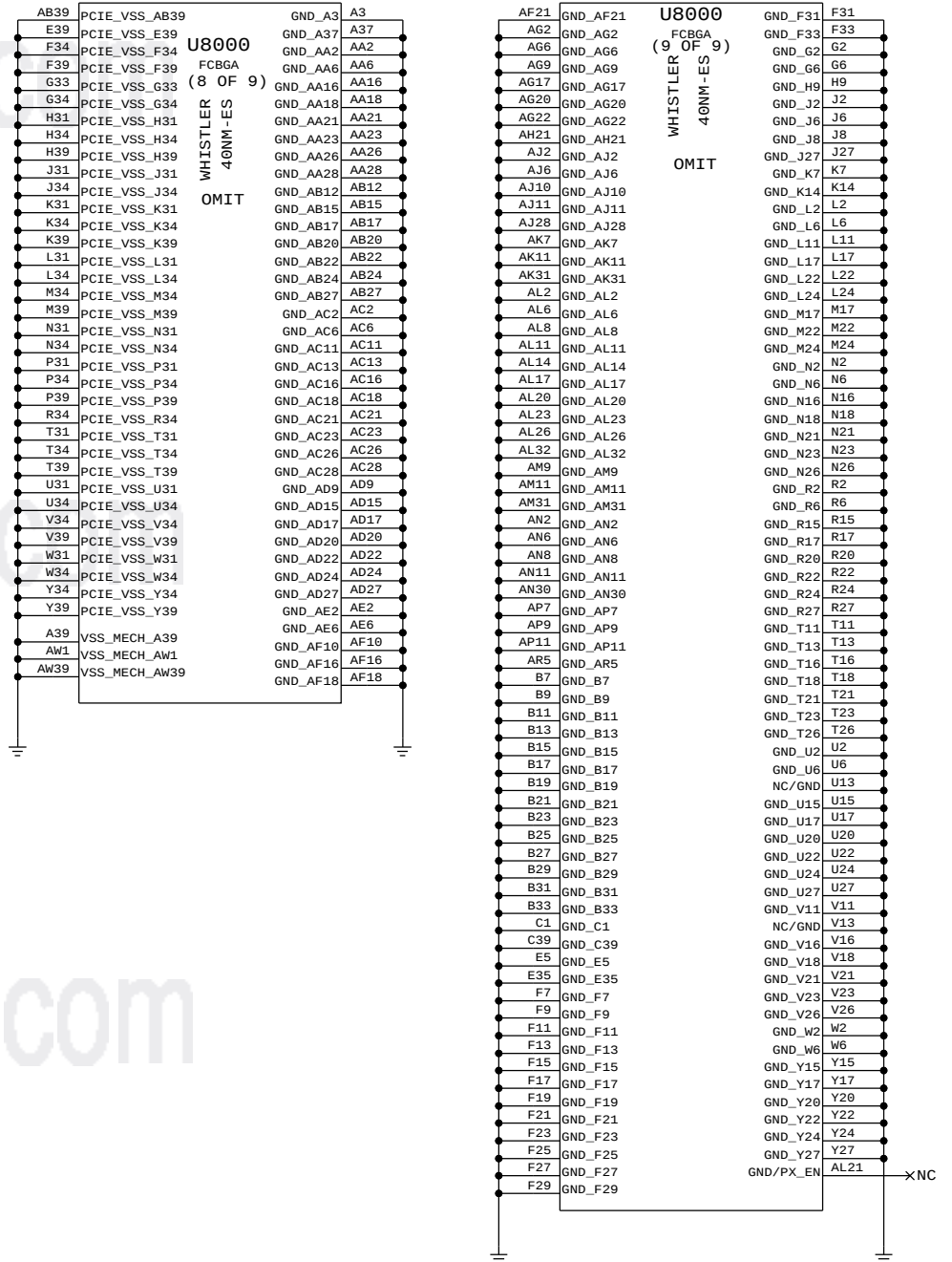
- #PP1V8_GPU_DP_AB
- #PP1V8_GPU_DP_CD
- #PP1V8_GPU_DP_EF
- #PP1V0_GPU_DP_AB
- #PP1V0_GPU_DP_CD
- #PP1V0_GPU_DP_EF

Signal aliases required by this page:

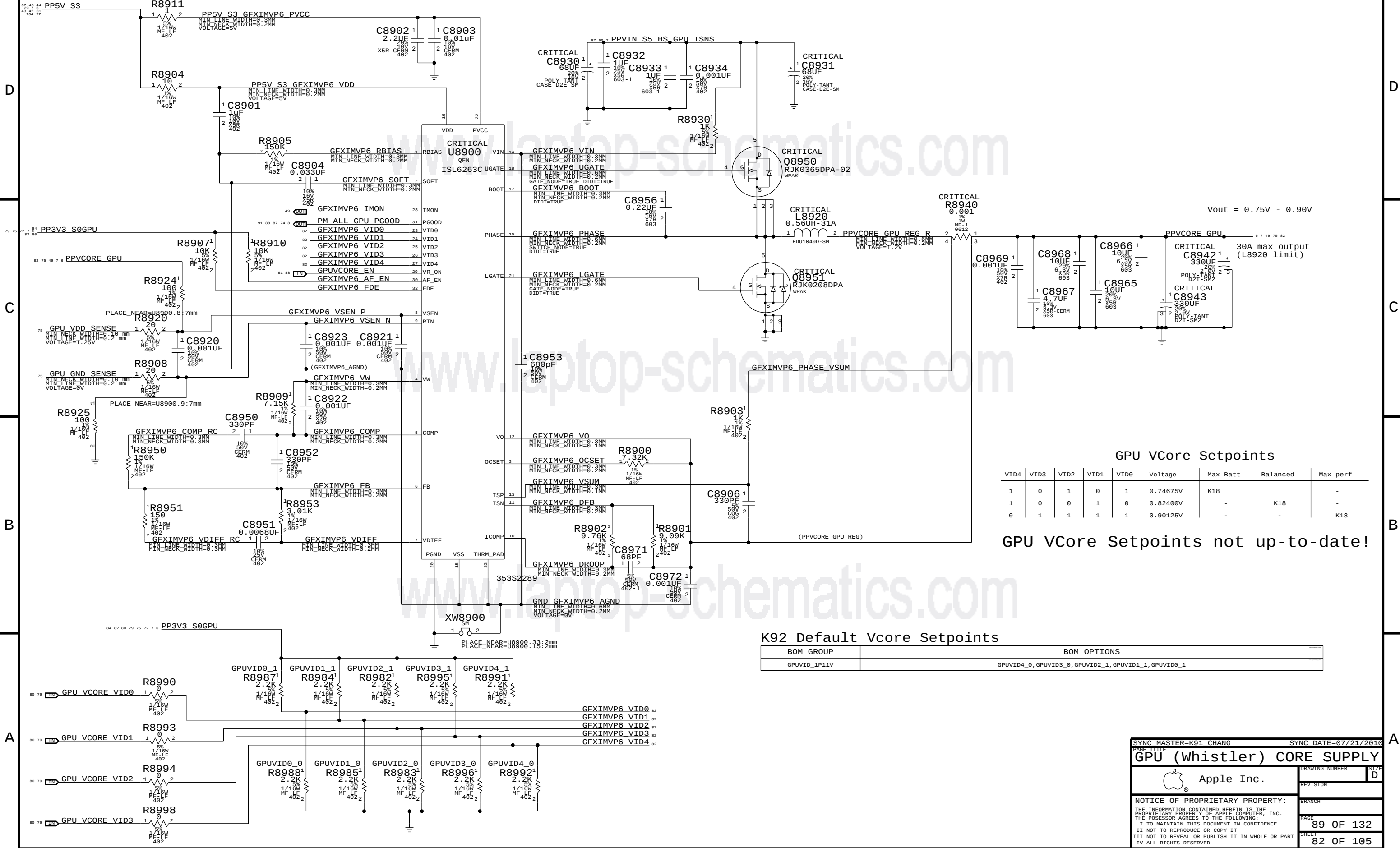
(NONE)

BOM options provided by this page:

(NONE)



GPU VCore Regulator



GPU VCore Setpoints									
VID4	VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf	
1	0	1	0	1	0.74675V	K18		-	
1	0	0	1	0	0.82400V	-	K18	-	
0	1	1	1	1	0.90125V	-	-	K18	

GPU VCore Setpoints not up-to-date!

K92 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_1P11V	GPUVID4_0, GPUVID3_0, GPUVID2_1, GPUVID1_1, GPUVID0_1

SYNC MASTER=K91 CHANG

SYNC DATE=07/21/2016

GPU (Whistler) CORE SUPPLY

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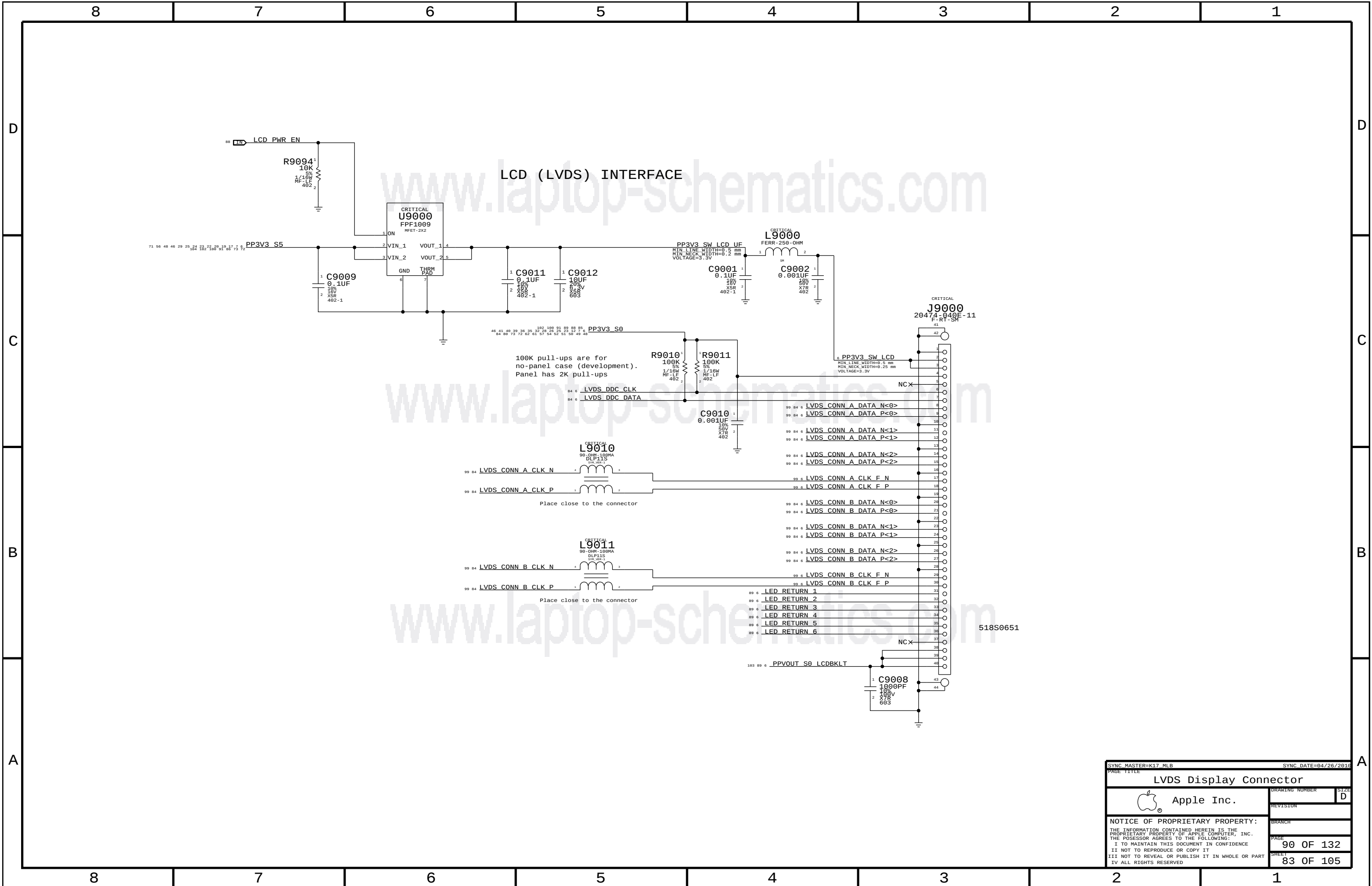
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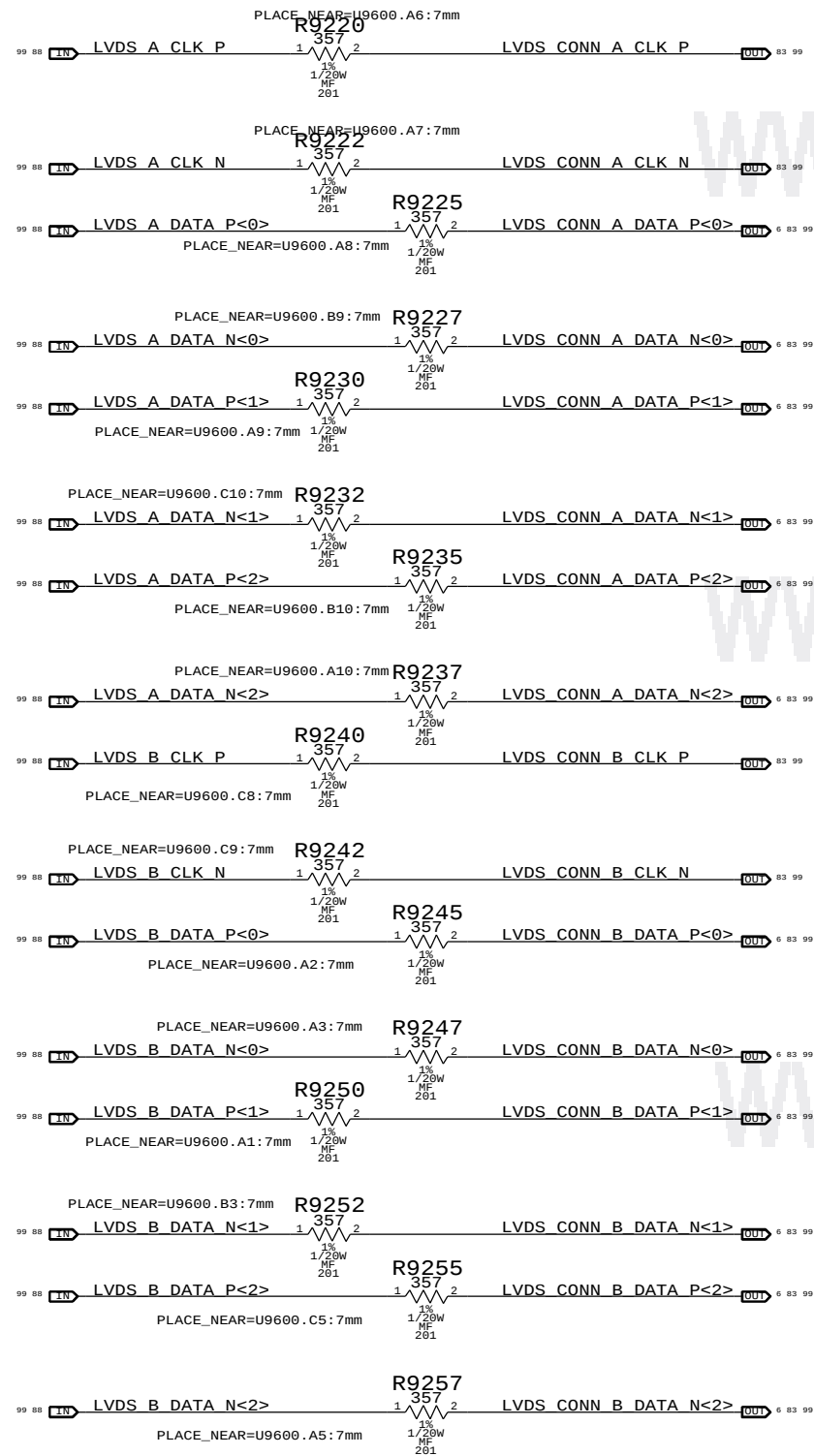
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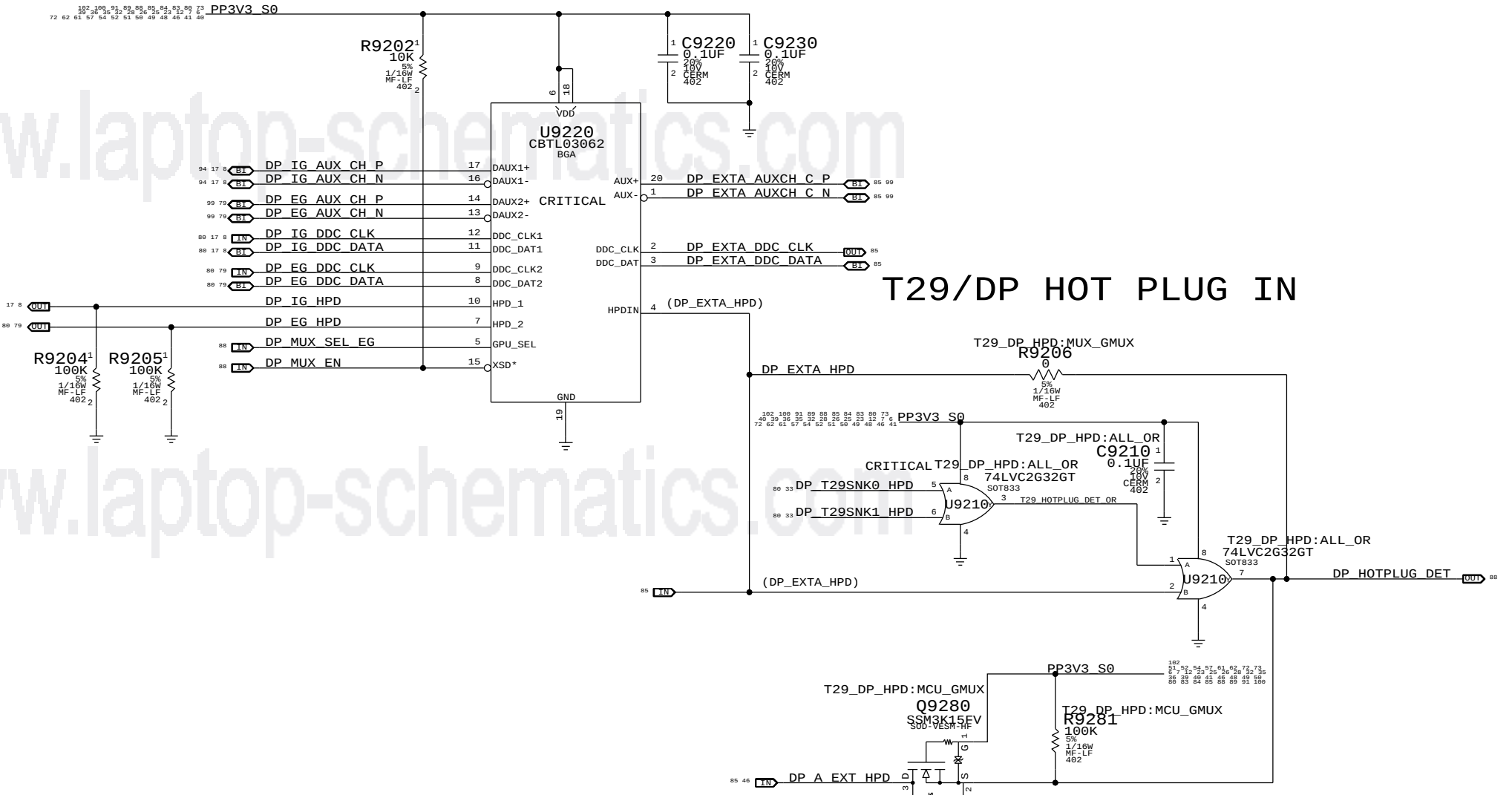


LVDS Transmitter Termination

All emulated LVDS outputs require this termination

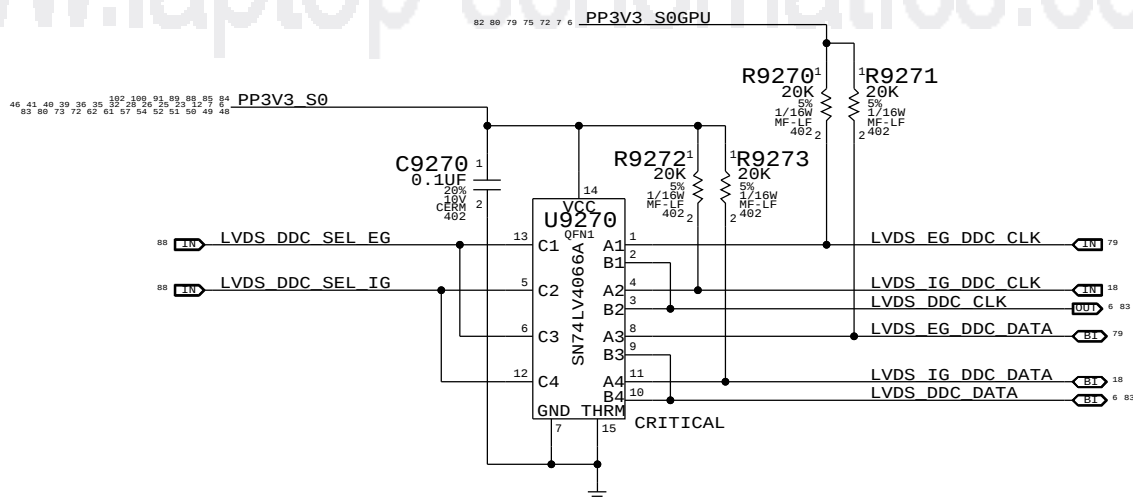


DP AUX, DDC, & HPD muxing to IG/EG

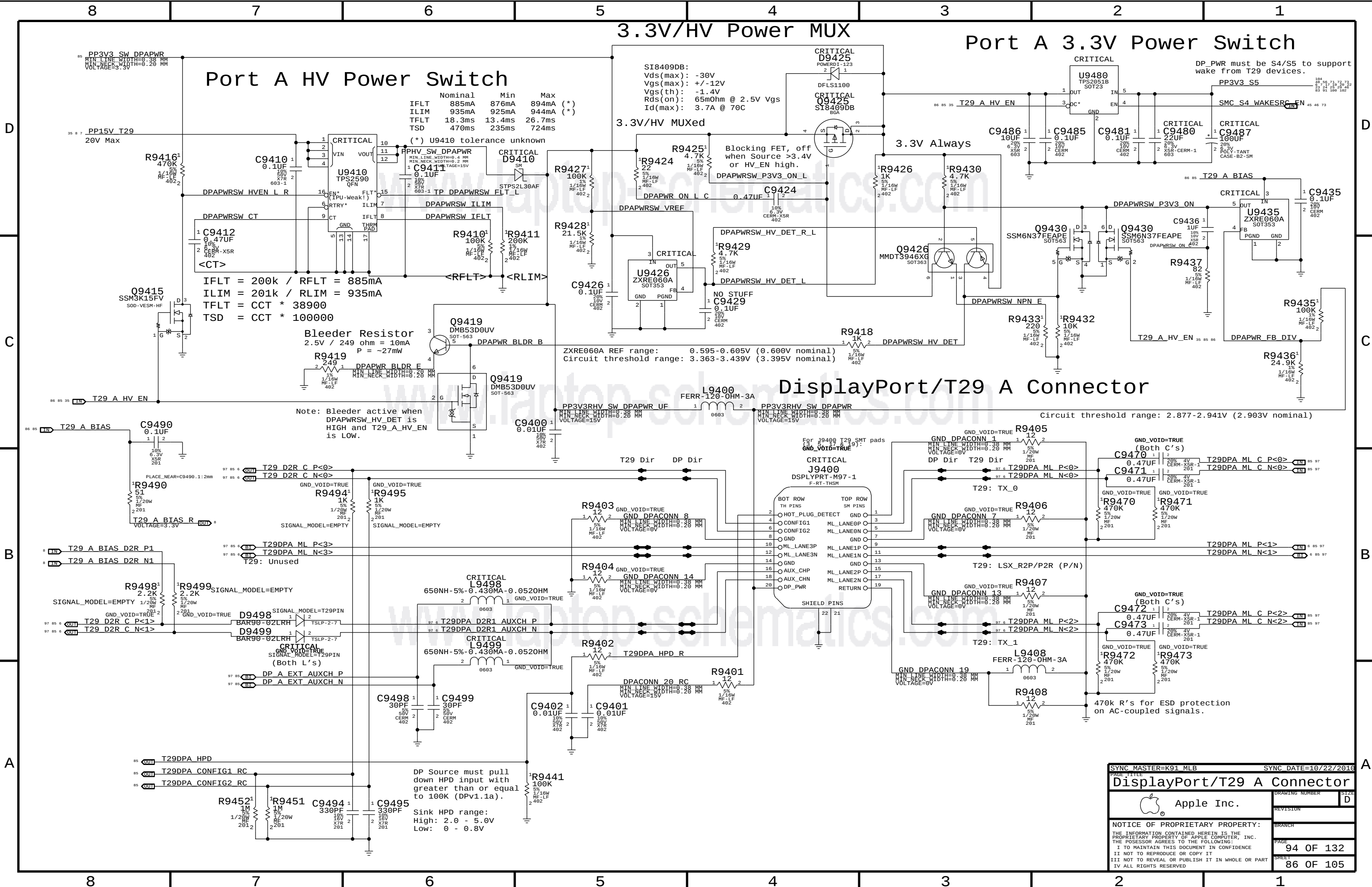


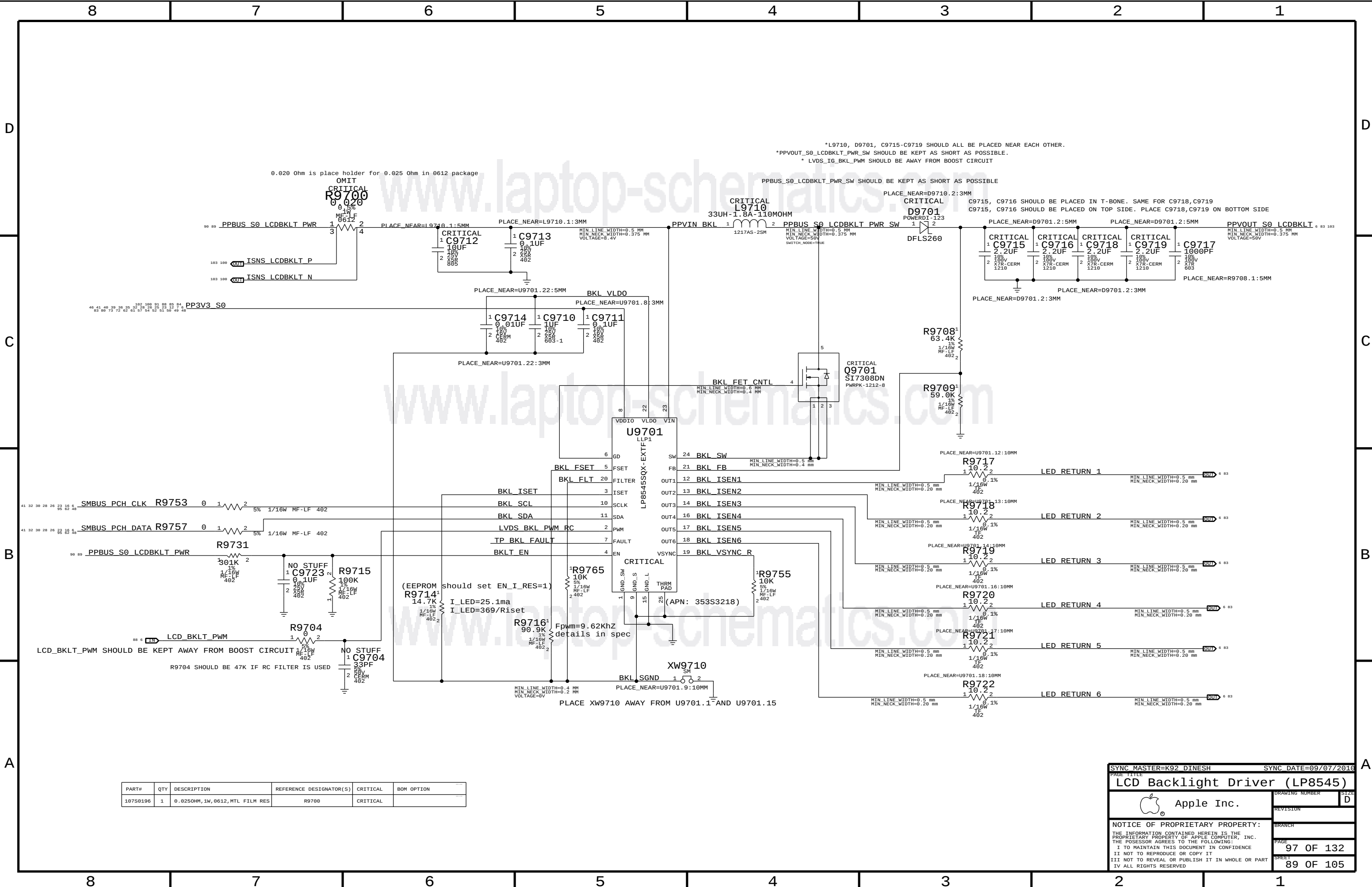
T29/DP HOT PLUG IN

LVDS DDC MUX



SYNC MASTER=K92 YUN		SYNC DATE=06/25/2016	
PAGE TITLE			
Muxed Graphics Support			
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
10750196	1	0.0250HM,1W,0612,MTL FILM RES	R9700	CRITICAL	

SYNC MASTER=K92 DINESH

SYNC DATE=09/07/2016

LCD Backlight Driver (LP8545)

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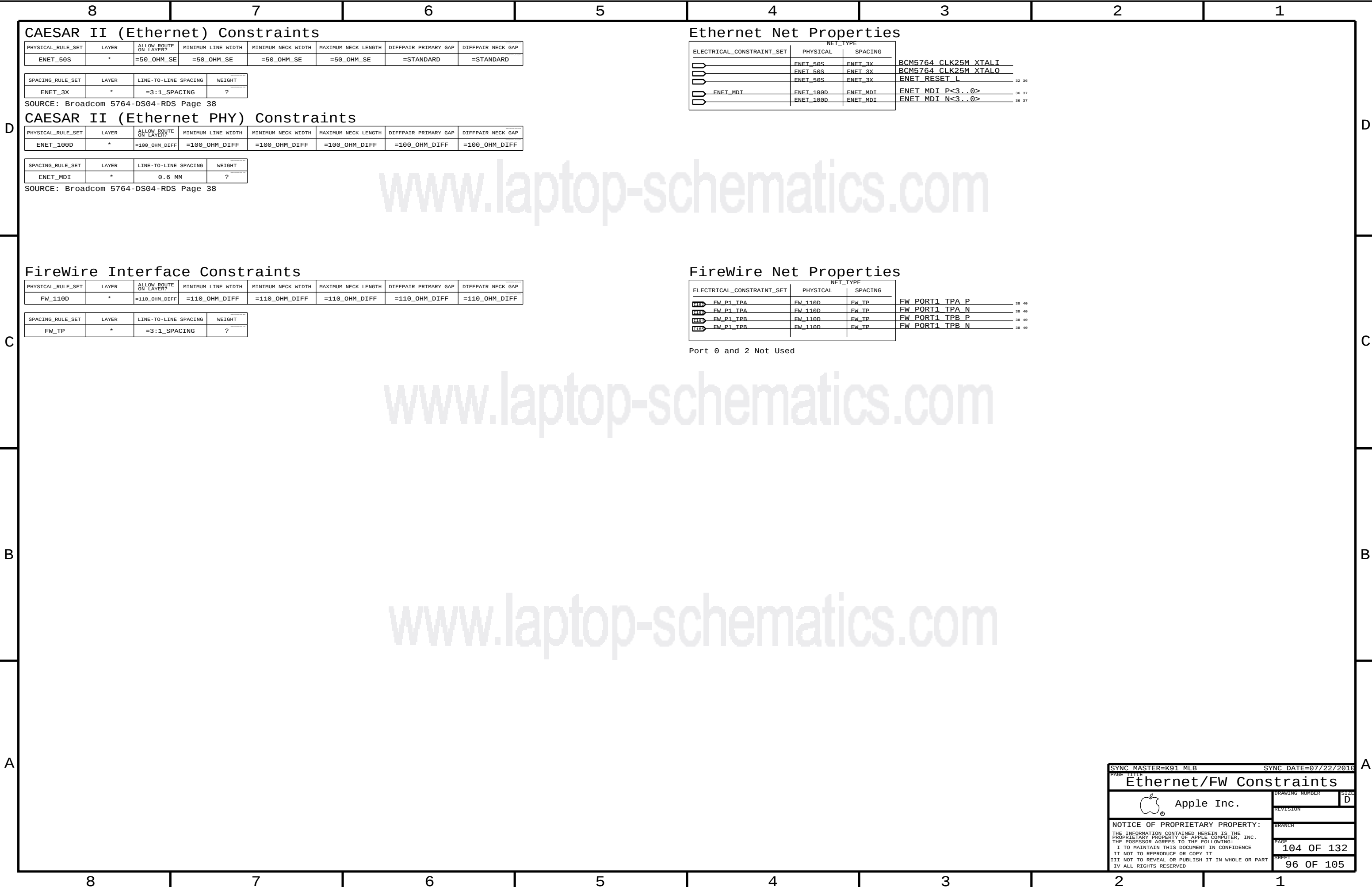
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GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=2x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=7x_DIELECTRIC	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?	DISPLAYPORT	TOP, BOTTOM	=4x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?	LVDS	TOP, BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DisplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	FR_A0_CLK	GDDR5_80D	GDDR5_CLK	FB A0 CLK P 76 77
	FR_A0_CLK	GDDR5_80D	GDDR5_CLK	FB A0 CLK N 76 77
	FR_A1_CLK	GDDR5_80D	GDDR5_CLK	FB A1 CLK P 76 77
	FR_A1_CLK	GDDR5_80D	GDDR5_CLK	FB A1 CLK N 76 77
	FR_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 A<8..0> 76 77
	FR_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 A<8..0> 76 77
	FR_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 ABI L 76 77
	FR_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 ABI L 76 77
	FR_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 RAS L 76 77
	FR_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 RAS L 76 77
	FR_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 CAS L 76 77
	FR_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 CAS L 76 77
	FR_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 WE L 76 77
	FR_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 WE L 76 77
	FR_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 CKE L 76 77
	FR_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 CKE L 76 77
	FR_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 CS L 76 77
	FR_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 CS L 76 77
	FR_A0_EDC0	GDDR5_45SE	GDDR5_FDC	FB A0 EDC<0> 76 77
1E2B0	FR_A0_EDC1	GDDR5_45SE	GDDR5_FDC	FB A0 EDC<1> 76 77
1E2B0	FR_A0_EDC2	GDDR5_45SE	GDDR5_FDC	FB A0 EDC<2> 76 77
1E2B0	FR_A0_EDC3	GDDR5_45SE	GDDR5_FDC	FB A0 EDC<3> 76 77
1E2B0	FR_A1_EDC0	GDDR5_45SE	GDDR5_FDC	FB A1 EDC<0> 76 77
1E2B0	FR_A1_EDC1	GDDR5_45SE	GDDR5_FDC	FB A1 EDC<1> 76 77
1E2B0	FR_A1_EDC2	GDDR5_45SE	GDDR5_FDC	FB A1 EDC<2> 76 77
1E2B0	FR_A1_EDC3	GDDR5_45SE	GDDR5_FDC	FB A1 EDC<3> 76 77
1E2B0	FR_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<0> 76 77
1E2B0	FR_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<1> 76 77
1E2B0	FR_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<2> 76 77
1E2B0	FR_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<3> 76 77
1E2B0	FR_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<0> 76 77
1E2B0	FR_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<1> 76 77
1E2B0	FR_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<2> 76 77
1E2B0	FR_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<3> 76 77
1E2B0	FR_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB A0 WCLK P<0> 76 77
1E2B0	FR_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB A0 WCLK N<0> 76 77
1E2B0	FR_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB A0 WCLK P<1> 76 77
1E2B0	FR_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB A0 WCLK N<1> 76 77
1E2B0	FR_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB A1 WCLK P<0> 76 77
1E2B0	FR_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB A1 WCLK N<0> 76 77
1E2B0	FR_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB A1 WCLK P<1> 76 77
1E2B0	FR_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB A1 WCLK N<1> 76 77
1E2B0	FR_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<7..0> 76 77
1E2B0	FR_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<15..8> 76 77
1E2B0	FR_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<23..16> 76 77
1E2B0	FR_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<31..24> 76 77
1E2B0	FR_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<7..0> 76 77
1E2B0	FR_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<15..8> 76 77
1E2B0	FR_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<23..16> 76 77
1E2B0	FR_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<31..24> 76 77
1E2B0	FR_AB_RESET	GDDR5_45R50SE	GDDR5_CMD	FB RESET L 76 77

GDDR5 FB B Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_P
	FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_N
	FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_P
	FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_N
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_A<8..0>
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_A<8..0>
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_ABT_L
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_ABT_L
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_RAS_L
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_RAS_L
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CAS_L
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CAS_L
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_WE_L
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_WE_L
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CKE_L
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CKE_L
	FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B0_CS_L
	FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB_B1_CS_L
	FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<0>
H33B	FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<1>
H33B	FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<2>
H33B	FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<3>
H33B	FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<0>
H33B	FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<1>
H33B	FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<2>
H33B	FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<3>
	FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<0>
H33B	FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<1>
H33B	FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<2>
H33B	FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<3>
H33B	FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<0>
H33B	FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<1>
H33B	FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<2>
H33B	FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<3>
	FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<0>
	FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<0>
	FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<1>
	FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<1>
	FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<0>
	FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<0>
	FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<1>
	FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<1>
	FB_B0_DQ_RYTF0	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<7..0>
	FB_B0_DQ_RYTF1	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<15..8>
	FB_B0_DQ_RYTF2	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<23..16>
	FB_B0_DQ_RYTF3	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<31..24>
	FB_B1_DQ_RYTF0	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<7..0>
	FB_B1_DQ_RYTF1	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<15..8>
	FB_B1_DQ_RYTF2	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<23..16>
	FB_B1_DQ_RYTF3	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<31..24>

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	LVDS_A_CLK	LVDS_850	LVDS	LVDS A CLK P 04 00
	LVDS_A_CLK	LVDS_850	LVDS	LVDS A CLK N 04 00
	LVDS_A_DATA	LVDS_850	LVDS	LVDS A DATA P<2..0> 04 00
	LVDS_A_DATA	LVDS_850	LVDS	LVDS A DATA N<2..0> 04 00
	LVDS_B_CLK	LVDS_850	LVDS	LVDS B CLK P 04 00
	LVDS_B_CLK	LVDS_850	LVDS	LVDS B CLK N 04 00
	LVDS_B_DATA	LVDS_850	LVDS	LVDS B DATA P<2..0> 04 00
	LVDS_B_DATA	LVDS_850	LVDS	LVDS B DATA N<2..0> 04 00
		LVDS_850	LVDS	LVDS CONN A CLK F P 6 03
		LVDS_850	LVDS	LVDS CONN A CLK F N 6 03
		LVDS_850	LVDS	LVDS CONN B CLK F P 6 03
		LVDS_850	LVDS	LVDS CONN B CLK F N 6 03
		LVDS_850	LVDS	LVDS CONN A CLK P 03 04
		LVDS_850	LVDS	LVDS CONN A CLK N 03 04
		LVDS_850	LVDS	LVDS CONN A DATA P<2..0> 6 03 04
		LVDS_850	LVDS	LVDS CONN A DATA N<2..0> 6 03 04
		LVDS_850	LVDS	LVDS CONN B CLK P 03 04
		LVDS_850	LVDS	LVDS CONN B CLK N 03 04
		LVDS_850	LVDS	LVDS CONN B DATA P<2..0> 6 03 04
		LVDS_850	LVDS	LVDS CONN B DATA N<2..0> 6 03 04

Whistler Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M 79 80
	GPU_CLK100M	CLK_SLOW_55S	CLK_SLOW	GPU_CLK100M 79 80
	LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS EG A CLK P 79 80
	LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS EG A CLK N 79 80
	LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS EG A DATA P<2..0> 79 80
	LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS EG A DATA N<2..0> 79 80
	LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC LVDS EG A DATA P<3> 79 80
	LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC LVDS EG A DATA N<3> 79 80
	LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS EG B DATA P<2..0> 79 80
	LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS EG B DATA N<2..0> 79 80
	LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC LVDS EG B DATA P<3> 79 80
	LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC LVDS EG B DATA N<3> 79 80
	DP_MI	DP_85D	DISPLAYPORT	DP EXTA ML C P<3..0> 79
	DP_MI	DP_85D	DISPLAYPORT	DP EXTA ML C N<3..0> 79
	DP_AUX_CH	DP_85D	DISPLAYPORT	DP EXTA AUXCH C P 84
	DP_AUX_CH	DP_85D	DISPLAYPORT	DP EXTA AUXCH C N 84
	DP_AUX_CH	DP_85D	DISPLAYPORT	DP EG AUX CH P 79
	DP_AUX_CH	DP_85D	DISPLAYPORT	DP EG AUX CH N 79

8	7	6	5	4	3	2	1
Board-Specific Spacing & Physical Constraints							
BOARD LAYERS				BOARD AREAS		BOARD UNITS (ALL OF MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA		MM	15.5.1
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP, BOTTOM	Y	0.185 MM	0.095 MM			
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.13 MM	0.13 MM			
45_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3, ISL4	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL9, ISL10	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2, ISL11	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.135 MM	0.135 MM		0.160 MM	0.160 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL9, ISL10	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.090 MM		0.190 MM	0.190 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9, ISL10	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.090 MM		0.230 MM	0.230 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2, ISL11	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.080 MM	0.080 MM		0.220 MM	0.220 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL4	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
110_OHM_DIFF	ISL9, ISL10	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
110_OHM_DIFF	ISL2, ISL11	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.							
8	7	6	5	4	3	2	1

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

NOTE: Based on K92 m1b stackup.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

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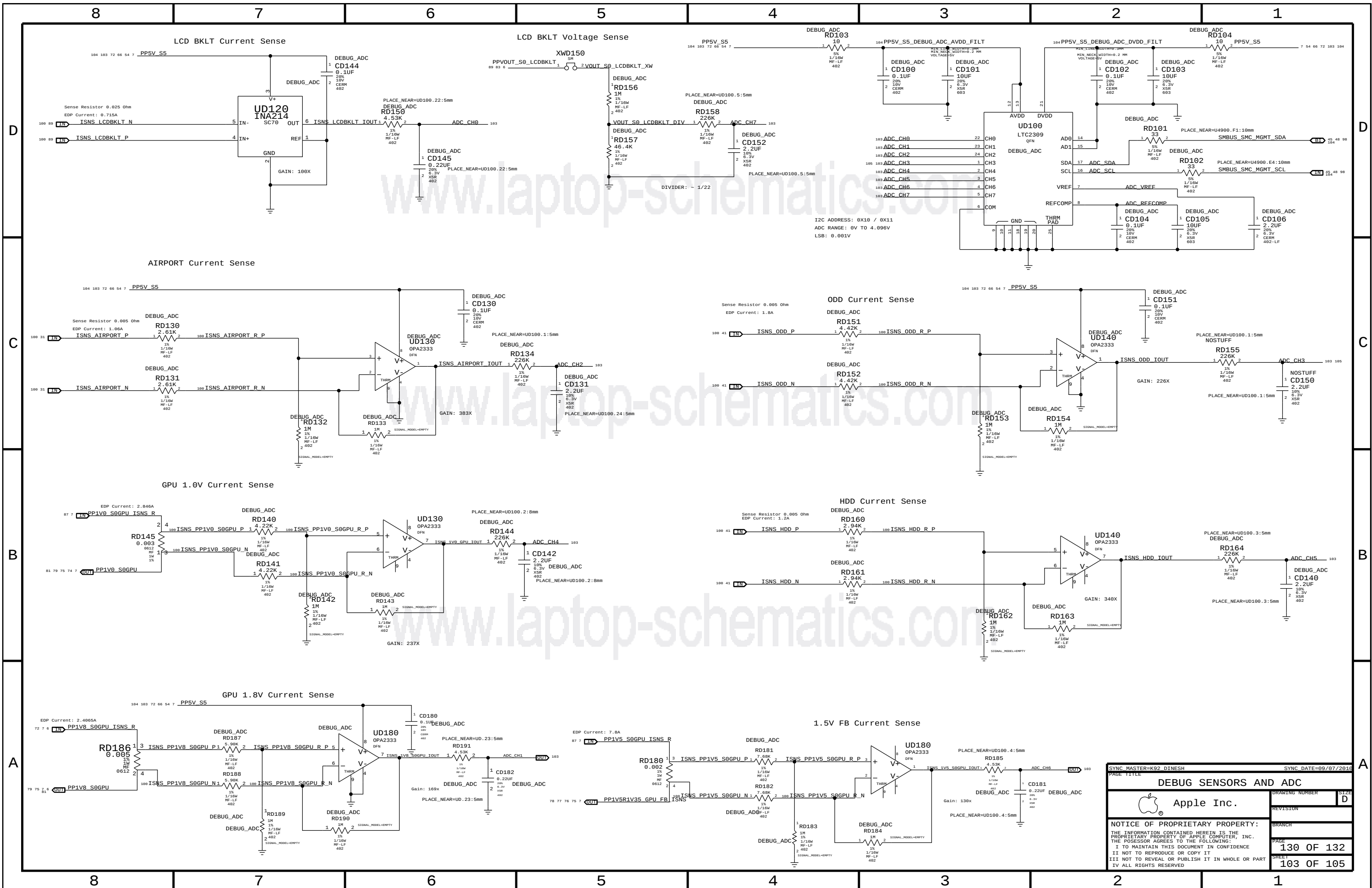
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PCH "S0" Rails

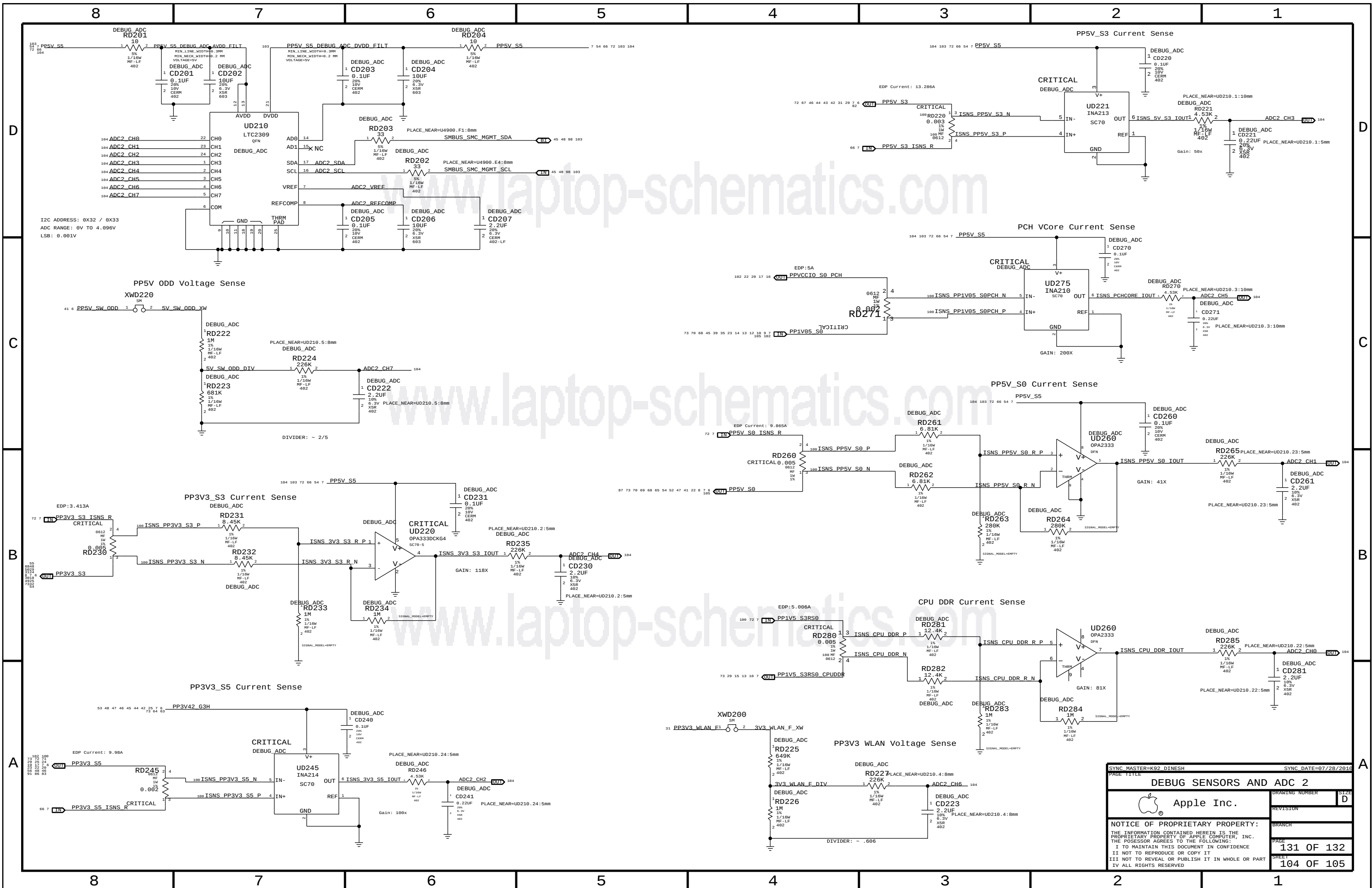
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